ISSN 2616-5767 Vol.6, Issue 11: 36-42, DOI: 10.25236/AJETS.2023.061106

Innovative design of signal separation device based on signal reconstruction method

Yifan Li[a], Hui Wang, Jiao Wu, Zhihua Li[b,*]

School of Information Science and Technology, Hangzhou Normal University, Hangzhou, Zhejiang, 311121, China
[a]35095758@qq.com, [b]zhihuali_e@163.com
[*]Corresponding author

Abstract: *In this paper, a signal separation device composed of adding circuit, level raising circuit, single-chip microcomputer control system, DDS module and post-amplifier circuit is designed, which can realize the process of signal reconstruction and separation after aliasing two different frequency signals. The phase offset is set by keyboard or step, and the waveform type, frequency and phase offset value of the two separated signals are displayed by on-board OLED in real time. The separation signal formed by signal reconstruction has stable voltage value, wide frequency range, fast processing rate and safe and reliable performance. This design provides a new idea for the innovative design of related signal separation circuit devices, and is worth of for reference.*

Keywords: *Adding circuit; Spectrum separation; Signal reconstruction*

1. Introduction

A mechanical system, a physical process or even a chemical process can usually obtain a signal through measurement methods such as sensors. However, in fact, the signal often contains multiple components, so the information contained in the signal can be very complex. In practical applications, we often need to decompose this complex signal from the overall expansion of the original sample into a series of sub-signal structures, which can provide richer and simpler information. This is called signal separation. The traditional filter has poor load capacity, unsatisfactory amplitude-frequency characteristics. What's more, there are also many restrictions on use of that. In this paper, an innovative signal separation method is proposed, which is based on the spectrum filtering analysis and signal reconstruction after that. In this way, the separated signal has small error with the original signal, wide frequency range circuit is stable and easy to be adjusted, and the accuracy of the instrument device is low.

This paper intends to design and make a signal separation device and the design principle is shown in Figure 1. Its function can realize dual-channel output 2-channel periodic signals A and B (frequency range: 20kHz ~100kHz, and fA < fB; The peak-to-peak value is 1V), and a mixed signal C is generated by an adder with a gain of 1, and signal C is divided into signals A' and B' thorough a separation circuit.

The design performance index of the device is set as follows.

(1) By making an adder with gain of 1, C=A+B is achieved;

(2) Signal A and B are sine waves, fA =50kHz, fB =100kHz. The device can correctly separate signals A' and B', and the peak-to-peak value is not less than 1V;

(3) Signal A and B are sine waves, whose frequency are an integer multiple of 10kHz. The signal A 'and B' can be correctly separated, and the peak-to-peak value is not less than 1V;

(4) Signal A and B are sine wave or triangular wave, respectively, and the frequency is an integer multiple of 5kHz. The signal A 'and B' can be correctly separated, and the peak-to-peak value is not less than 1V;

(5) Signals A and B are sine waves, and fB is an integer multiple of fA. The initial phase difference between signal B' and A' can be set and controlled, the range is 0°~180°, the setting resolution is 5°, and the absolute value of the error is not more than 5°.

ISSN 2616-5767 Vol.6, Issue 11: 36-42, DOI: 10.25236/AJETS.2023.061106

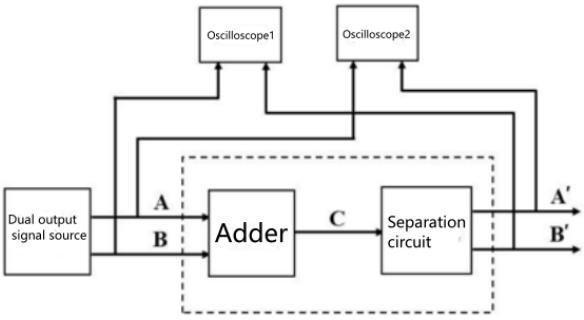

Figure 1: Design schematic principle

2. Scheme Design

With low noise, high precision speed operational amplifier (A(VCL) > -5) and a gain bandwidth of 63MHz, OP37 is used in this paper for adding circuit. Op37 not only has the characteristics of low offset voltage and drift of OP-07, but also has higher speed and lower noise. Low noise and high gain make the low level signal get accurate high gain amplification. The frequency range of the detection signal of the device is 20khz~100kHz, which requires a higher bandwidth after calculation, so OP37 is finally selected to make an adding circuit.

Aiming at the level raising circuit, the aliasing signal is processed by it. When raised it to no negative voltage, it is convenient for the later stage to access STM32 for AD sampling. The two-stage NE5532 amplifier circuit is selected. NE5532 is a high-performance low noise dual operational amplifier (dual op-amp) integrated circuit. Similar to many standard operational amplifiers, it has lower noise, excellent output driving capability, quite high small signal bandwidth (gain bandwidth up to 10MHz) and wide voltage and power range.

AD acquisition

(1) High-speed AD module AD7606 performs AD acquisition. AD7606 is a 16-bit, 8-channel synchronous sampling chip with a sampling rate of up to 200KSPS per channel[1].

(2) STM32 on-board AD implements sampling. Its maximum sampling rate can theoretically reach 851K, and STM32 ADC module usually includes a number of units, of which, also known as core unit, is ADCx(x represents the number). Each ADC unit can convert multiple analog sampling channels and supports multi-channel conversion, with ADC1/ADC2 supporting up to 16 channels and ADC3 supporting up to 18 channels.

Considering that this device is a single signal acquisition and has high frequency requirements, the on-board AD can perfectly meet the requirements, and the spectrum acquisition range can be adjusted at any time to facilitate the subsequent initial phase setting, so STM32 on-board AD is selected for sampling.

Output module

(1) DAC8563 is a low-power, voltage-output, dual-channel, 16-bit digital-to-analog converter with an output analog bandwidth of 100KHz.

(2) STM32 DAC module (digital/analog conversion module) is a 12-bit digital input and voltage output type DAC. The DAC can be configured in 8-bit or 12-bit mode, or can be used with a DMA controller, and the data can be set to left-justified or right-justified when the DAC is operating in 12-bit mode. The DAC module has 2 output channels, each with a separate converter. In dual DAC mode, the two channels can be converted independently, or the two channels can be converted simultaneously and the output of both channels can be updated synchronously.

(3) The AD9833 is a DDS module, whose default on-board is 25MHz (25ppm accuracy) imported active crystal oscillator, the stepping accuracy is 0.1Hz. It can access the external clock reference through the tee, have higher frequency resolution, can output frequency, phase programmable amplitude of about 0.6VPP sine wave and triangle wave[2].

The bandwidth of DAC8563 is small, which does not meet the requirements of the detection range,

ISSN 2616-5767 Vol.6, Issue 11: 36-42, DOI: 10.25236/AJETS.2023.061106

and the DAC of STM32 cannot achieve a high frequency, so its output sine wave frequency is not high. The waveform of high-frequency sine wave DAC with too few output points will be distorted, while the DDS module can avoid this situation, and its output speed is fast and the bandwidth can meet the requirements. To sum up, two AD9833 are selected in this scheme to output separation signals A' and B' respectively.

At the same time, since the AD9833 module can control the phase of the output waveform through programming, this paper chooses the DDS module to shift the phase directly. The two AD9833 are connected to the same external clock so that the initial phase of the output waveform is same.

3. Theoretical analysis and calculation

In this paper, the signal is distinguished based on the following signal separation principle, that is, the waveform array sampled by ADC is analyzed to obtain the spectrum amplitude array. According to the spectrum amplitude array, the characteristic spectrum of the two signals is obtained, which is further distinguished according to the spectrum characteristics of the triangular wave and sinusoidal wave.

According to the sampling theorem, the sampling frequency is set to 3~5 times of the maximum frequency of 100kHz. Considering the need to analyze the third harmonics of the triangular wave, the sampling rate is set to 720k.

Using the library function to implement 1024-point FFT, we get an output array with the higher 16 bits as the imaginary part and the lower 16 bits as the real part.

The operation of separating different frequency signals is as follows: the output array is decomposed into real part (X) and imaginary part (Y), and then the formula sqrtv(X*X, Y*Y) is used to calculate the amplitude of each harmonic. By searching the processed array, the maximum value and its array subscript can be found. In this way, the fundamental frequency of a signal can be obtained. By searching the array again, and skipping the maximum value subscript that has been found, the second maximum value and its array subscript is found and the fundamental frequency of the second signal is obtained.

$$\text{Frequency per point} = \text{corresponding subscript} * \text{resolution}$$

$$\text{Resolution} = \text{sampling frequency/sampling number}$$

Two kinds of waveforms are distinguished as follows: according to the waveform characteristics, the sine wave has only fundamental wave component and basically no harmonic component; In addition to the fundamental wave component, the triangular wave also has harmonic components of 3, 5 and 7, and the three times harmonic component is 1/9 of the fundamental wave component. The three times harmonic component are found in the amplitude value array to distinguish the triangular wave from the sine wave.

The frequency leakage caused by the limitation of measurement timing accuracy and the zero-filling operation leads to the attenuation of the amplitude of the correct frequency points in the spectrum and the stray frequency points around the correct frequency points[3].The third harmonic of triangular wave is smaller than the theoretical value, which is 1/10 of the fundamental wave component. Because of the fence effect, the obtained frequency has some error, and this scheme reduces the error by improving the resolution.

Phase shift is carried out by AD9833 module. The AD9833 is composed of an adder and a phase register, and the phase register is increased by the step of each clock. The output of the phase register is added with the phase control word. Then the result is input to the sinusoidal query table address. The sine query table contains the digital amplitude information of A periodic sine wave, and each address corresponds to a phase point within 0~360° of the sine wave. The query table maps the phase information of the input address into the sine wave amplitude, and drives the output analog of the D/A converter.

4. Circuit and programming

Figure 2 shows the overall design structure.

ISSN 2616-5767 Vol.6, Issue 11: 36-42, DOI: 10.25236/AJETS.2023.061106

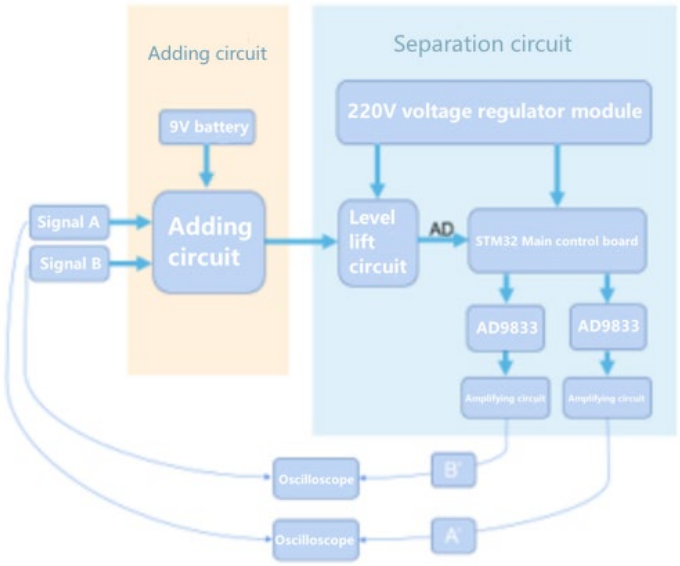

Figure 2: Overall hardware design drawing

Figure 3 shows the adding circuit, which is built by OP37, powered separately by a 9V alkaline battery and amplified by input from the reverse side.

$$A_u = \frac{R1}{R3} * U_1 + \frac{R1}{R4} * U_2$$

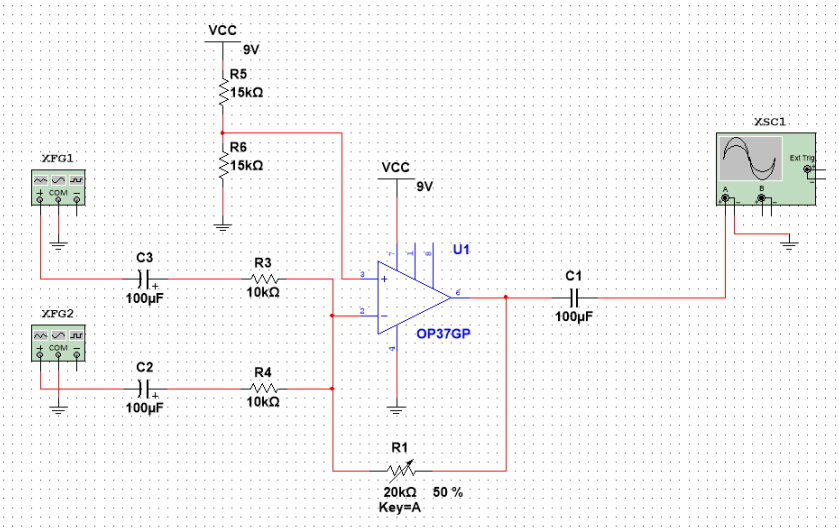

Figure 3: Adding circuit

The separation circuit takes the main control board as the core to recognize the waveform. The front end is the level raising circuit, and the back end is the waveform generating circuit and amplifying circuit. The lifting circuit uses NE5532, the waveform generating circuit uses AD9833, and the final amplifying circuit uses OP37.

Figure 4 shows the level lift circuit, which is connected to the output end of the adding circuit. The main function of the circuit is to adjust the aliasing signal, so that the signal can be connected to STM32 for AD sampling. The circuit magnification is adjusted by adjusting the resistance values of R4 and R7.

$$V_{\text{lift}} = V_{cc} * \frac{R3}{R2+R3}$$

ISSN 2616-5767 Vol.6, Issue 11: 36-42, DOI: 10.25236/AJETS.2023.061106

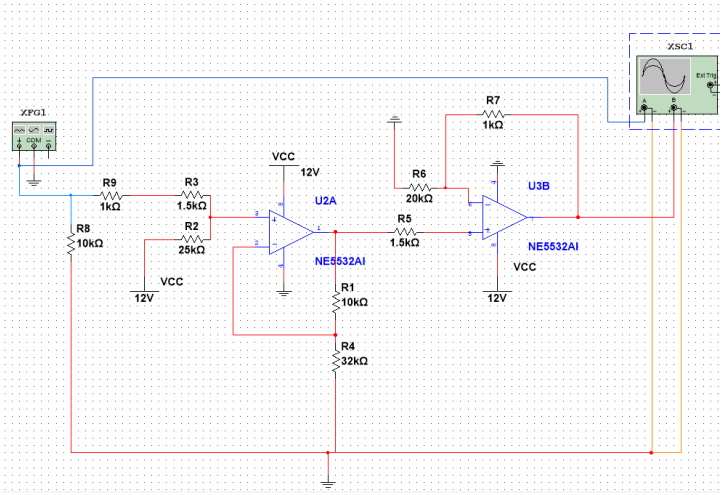

Figure 4: Level lift circuit

Figure 5 shows the post-amplifier circuit of the AD9833. Since the peak value of the signal peak output through the AD9833 is fixed at 600mV, in order to facilitate the viewing of the waveform, OP37 is used to build the amplifier circuit, so that the peak value of the final output signal peak is more than 1V.

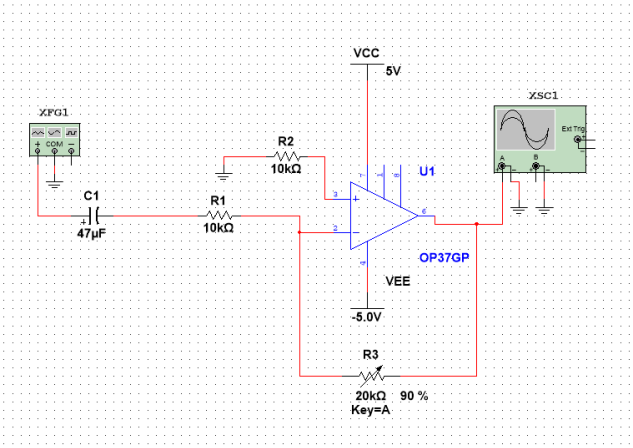

Figure 5: Post-amplifier circuit

Figure 6 shows the overall process flow chart.

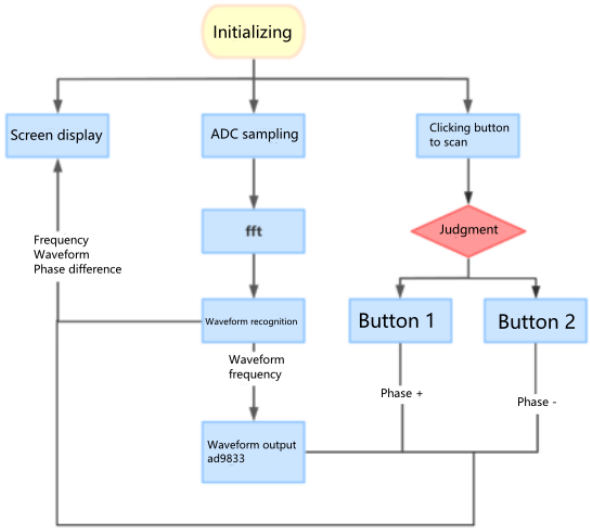

Figure 6: The overall process flow

ISSN 2616-5767 Vol.6, Issue 11: 36-42, DOI: 10.25236/AJETS.2023.061106

For waveform recognition, the output signal C of the adding circuit passes through the level raising circuit, uses the STM32F03 main control board to perform ADC sampling, performs FFT calculation on the collected array, and obtains a series of data. The data is processed, the fundamental waves of the two signals are found. Then, the third harmonic values in the data are compared according to the Fourier expansion coefficient of the triangular wave, combined with the hardware debugging data, the waveform recognition of the arbitrary mixing and addition of the double-channel signal, triangular wave and sine wave is finally realized.

For waveform output, DDS chip uses AD9833, according to the waveform recognition obtained by the dual signal waveform and the signal frequency obtained by FFT, by using their own functions to modify the control word of AD9833, the signal output of different frequencies and waveforms is realized.

In order to make the output signal and the corresponding signal stably display at the same frequency, by observing oscilloscope, it is found that the output signal frequency of AD9833 would have a small error, so the device fitted and corrected the frequency value transmitted to the AD9833 according to the actual data. When the AD9833 outputs sine wave, the fixed output peak value is 60mVpp, so the amplifier circuit is added behind it, which ensures that the final output signal peak value is not less than 1V.

5. Test scheme and the result

In the adding circuit, since the input has two signals A and B, when the two signal frequencies are different, the gain of the circuit will change with the frequency variation. Thus, the gain can be observed by input two signals with the same frequency.

In the level lifting circuit, the input sine wave with a peak value of 2V (bipolar) changes the amplification factor and the lifting voltage by adjusting the resistance value, so that the output voltage has no negative signal and the maximum value is less than 3.3V.

A series of calculations, such as FFT, are performed on the waveform array sampled by ADC to obtain the fundamental frequencies of the two signals, which are further distinguished according to the spectrum characteristics of the triangular wave and sinusoidal wave. All the circuits are connected, and two signals of different frequencies are input according to the expected requirements, and then observing whether the two signals are successfully separated through the oscilloscope.

The test results are as follows.

Table 1: Adding circuit

Test data: A+B = C				
The peak value of A Peak/V	A frequency/Hz	The peak value of B Peak/V	B frequency/Hz	The peak value of C Peak/V
1	20k	1	20k	2.04
	40k		40k	2.08
	50k		50k	2.02
	60k		60k	2.03
	80k		80k	2.07
	100k		100k	2.04

Table 1 shows the test data of the adding circuit. It can be seen from the table that A+B = C, that is, the gain is 1.

Table 2 shows the measurement data of the whole circuit.

Table 2: Integral measurement data

The peak value of A Peak/V	A frequency /Hz	The peak value of B Peak /V	B frequency/Hz	The peak value of A' Peak /V	A' frequency /Hz	The peak value of B' Peak /V	B' frequency /Hz
1	20k	1	60k	1.24	20000.3	1.25	60000.2
	25k		75k	1.24	25000.2	1.24	75000.3
	30k		90k	1.22	30000.3	1.23	90000.1
	50k		100k	1.21	50000.1	1.23	100000
	40k		80k	1.21	40000.2	1.18	80000.2
	30k		60k	1.18	30000.3	1.19	60000.3
	20k		40k	1.18	20000.3	1.18	40000.3

ISSN 2616-5767 Vol.6, Issue 11: 36-42, DOI: 10.25236/AJETS.2023.061106

It can be seen from Table 2 that the peak values of A 'and B' peaks are not less than 1V, meeting the requirements of the design; The frequency of A 'and B' is basically the same as that of A and B, and the signal is successfully separated and displayed.

6. Conclusion

The signal separation device designed in this paper has reached the expected design expectation. In terms of function, the phase difference of the output signal can be set by the buttons, and the waveform type and frequency of the two signals can be displayed on the screen. The whole system is stable and reliable. The core technology of this design is the spectrum identification process, by searching the spectrum array to find two maximum values in turn, which is the signal fundamental wave. When the frequency difference between A and B is three times, it is easy to make a mistake when comparing the three times harmonics, which will affect the recognition result. The solid program makes a special treatment for the triple frequency case, saves the maximum value, and takes two sub-maximum value again, which is the correct third harmonic. When the AD9833 output signal, considering that the difference accuracy of the collected signal is 5k, the obtained signal is corrected to a multiple of 5 to ensure that the output signal error is extremely minimal.

In the future, we will consider choosing the main control board with higher frequency, such as FPGA, and adding the software phase-locked loop to lock the waveform phase so that the waveform of the same frequency observation is more stable, which can further improve the accuracy of the system output signal and its stability.

Acknowledgment

Project source: 2023 National Undergraduate Electronics Design Contest.

References

[1] Jiang Siyu, Wang Bin, Yu Longhai, et al. Design and implementation of multi-channel Data sampling System based on FPGA+AD7606 [J]. Electronic Design Engineering, 2022, 30(22): 103-107.
[2] Shen Qinghua. Design of high-precision function Signal Generator based on AD9833 [J]. Electronic Testing, 2021(19): 38-40.
[3] Chen Peng, Zhao Shaomei, Chen Qin, etc. A Multifrequency Real Signal Frequency Estimation Algorithm for Spectrum Leakage Correction [J]. Journal of Vibration and Shock, 2021, 40(15):107-113.