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A Review of Recent Progress on Graphene Fabrication through Pyrolysis of Silicon Carbide

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Abstract: *Graphene, renowned for its exceptional electromagnetic and thermal properties, has found widespread applications across diverse fields, including sensors and electronic transistors. The performance of graphene hinges on the quality of the material, thereby dictating its suitability for various applications. Despite its promising attributes, current production techniques fail to satisfy the demands, particularly in high-performance applications like transistors. Since the pioneering isolation of graphene, significant strides have been made in the epitaxial growth of graphene on silicon carbide over nearly two decades. This method is recognized as one of the most auspicious approaches for achieving large-area, uniform, and controllable high-quality graphene production. This paper aims to consolidate the existing methodologies for graphene production via silicon carbide epitaxy, delineate their respective advantages and drawbacks, and proffer insights into potential avenues for future development.*

Keywords: *graphene, silicon carbide, pyrolysis*

1. Introduction

Since its successful discovery and isolation, graphene has been the subject of extensive investigation regarding its properties and applications. Over nearly two decades of research, it has been established as a genuine two-dimensional semiconductor devoid of a bandgap, exhibiting electron behavior akin to relativistic (Dirac) electrons [10]. Graphene demonstrates exceptional electronic characteristics [1-3], boasting a high charge carrier mobility of up to $10^6\ cm^2 \cdot V^{-1} \cdot s^{-1}$ [4], surpassing 4-6 $mA \cdot \mu m^{-1}$ in current stability [5,6]. Additionally, it can endure extraordinarily high current densities (exceeding those of copper by a factor of a million) [6], exhibits high-temperature stability, and possesses high thermal conductivity [7]. Furthermore, it showcases novel magnetic transport properties, room-temperature ballistic transport characteristics, complete impermeability to any gas, and facile chemical functionalization [9,10].

The application areas of a material are inherently determined by its properties. Owing to graphene's exceptional electromagnetic characteristics, both research and industrial advancements in graphene have undergone rapid development over the past two decades. Particularly in the post-Moore's Law era, graphene demonstrates promising potential across various domains such as single-molecule gas sensing, spintronics, quantum computing, and terahertz oscillator devices. Moreover, the integration of graphene with insulators to form Schottky junctions holds significant theoretical promise as an innovative successor to silicon, offering an alternative channel material to silicon MOSFETs in integrated circuits.

S. Hertel et al. showcased the fabrication of transistors boasting high on/off ratios by employing epitaxial graphene on 6H-SiC (0001). In this setup, graphene fulfills the roles of the source, drain, and gate, whereas the silicon carbide substrate functions as the semiconductor transistor channel. This pioneering approach validated the unipolar field-effect transistor (FET) at the interface of graphene and silicon carbide (see Fig. 1), akin to metal-semiconductor FETs.

Y.-M. Lin et al. demonstrated the production of FETs with cutoff frequencies reaching up to 100 GHz in the radio-frequency spectrum, using 2-inch graphene wafers (refer to Fig. 2). Additionally, in the realm of resistance standards, graphene samples grown on silicon carbide have exhibited superior resistance accuracy at elevated temperatures compared to conventional GaAs heterostructures. However, in various graphene applications, particularly in integrated circuits, there exists a pressing demand for enhanced material quality and larger areas. Presently, graphene materials suitable for manufacturing and application must adhere to criteria encompassing uniform large-scale production, superior quality, cost-effectiveness, and optimal growth conditions during fabrication. The inherent lack of a bandgap in graphene (Eg=0 eV) severely constrains current modulation in graphene FETs, leading to bipolar behavior. This phenomenon results in macroscopic graphene transistors conducting substantial current even at their minimum conductivity point (commonly referred to as the Dirac point or charge neutrality point), thus impeding their potential as a viable replacement for silicon MOSFETs in forthcoming CMOS-type logic circuits.

The method of preparation plays a pivotal role in determining the quality of graphene, thereby influencing its potential applications. Initially synthesized in 2004 through mechanical exfoliation, graphene production via this method offers high quality at a low cost. However, it is limited to small-scale production, typically within the range of 10 μm, posing challenges for achieving large-scale applications. Current approaches like Chemical Vapor Deposition (CVD) and graphite exfoliation encounter hurdles in meeting the demands of scalable graphene production. Ongoing research by Florian Wendler, J. Hass, and others aims to realize uniform, high-quality, large-area graphene growth on insulating substrates, eliminating the need for substrate transfer as required in CVD methods. Epitaxial techniques employing 6H-SiC and 4H-SiC hold promise in meeting these criteria. Epitaxial graphene has demonstrated remarkable carrier mobility of up to 27,000 $cm^2 \cdot V^{-1} \cdot s^{-1}$[6], while suspended graphene exhibits even higher mobility, reaching up to 200,000 $cm^2 \cdot V^{-1} \cdot s^{-1}$[7-9]. The epitaxial graphene preparation technique utilizing silicon carbide presents substantial advantages for future industrial applications. Silicon carbide's well-ordered crystal structure and wide bandgap semiconductor properties make it suitable for high-voltage and high-power electronics. Furthermore, its processing technology in the electronics domain is compatible with silicon, and its material properties are extensively studied. When graphene interfaces with silicon carbide, a Schottky barrier is formed, where graphene behaves as a metal while silicon carbide acts as a barrier, impeding significant charge carrier exchange. This interface can be engineered to establish electron-transparent Ohmic contacts, rendering it ideal for rapid and efficient switching applications.

The epitaxial graphene production process on silicon carbide involves the sublimation of SiC in a vacuum, yielding four gaseous derivatives initially: silicon (Si), Si_2C, SiC_2, and SiC. Notably, silicon exhibits a significantly higher vapor pressure compared to the other derivatives. By precisely controlling experimental parameters, such as lower vacuum levels and relatively higher temperatures, a larger quantity of silicon atoms preferentially sublime from the SiC substrate. Consequently, the SiC surface experiences a notable enrichment in carbon atoms due to the substantial deposition of silicon. Under elevated temperatures, these carbon atoms undergo restructuring with minimal energy, forming carbon materials characterized by sp^2 bonds.

From both thermodynamic and kinetic viewpoints, epitaxial graphene production on silicon carbide involves two concurrent chemical processes: (1) The cleavage of Si-C bonds (sp^3), causing silicon atoms with higher vapor pressure to evaporate from the substrate surface; (2) The establishment of C-C bonds (sp^2), wherein liberated carbon atoms diffuse, nucleate, and progressively grow on the SiC surface at elevated temperatures, ultimately forming hexagonal layers of carbon atoms and resulting in graphene formation.

2. Development process

Since the groundbreaking work by Berger and de Heer in 2004, who pioneered the epitaxial method for producing graphene on silicon carbide substrates [11,12], researchers have persistently explored various preparation techniques over the past decade. The aim has been to enhance graphene quality and simultaneously mitigate production costs. In this review, we comprehensively summarize and evaluate the existing epitaxial methods utilized for graphene production on silicon carbide substrates.

2.1 Thermal environment

Presently, academic research on epitaxial graphene on silicon carbide substrates predominantly centers around two distinct thermal decomposition environments: ultra-high vacuum (UHV) and confinement controlled sublimation (CCS).

During epitaxial graphene fabrication on silicon carbide substrates under ultra-high vacuum conditions, several challenges arise. These include lower formation temperatures, limited area coverage, uneven layer distribution, and higher defect densities. These issues stem primarily from the accelerated sublimation rate of silicon atoms, which surpasses their equilibrium state, resulting in excessively rapid material growth and complicating thickness control. Furthermore, this epitaxial approach necessitates stringent vacuum conditions and extended processing times, consequently increasing material preparation costs.

In 2006, J. Hass et al. achieved exceptional quality epitaxial graphene on 4H-SiC and 6H-SiC (0001) substrates within ultra-high vacuum conditions, showcasing compatibility with wafer-scale semiconductor processing [8]. Concurrently, Walt de Heer et al. generated continuous, two-dimensional graphene films, merely 1-2 carbon atoms thick, on silicon carbide surfaces under high vacuum conditions at 1300 ℃. The Confinement Controlled Sublimation (CCS) environment for thermal decomposition of SiC to produce graphene primarily revolves around optimizing the process to decelerate the sublimation rate of silicon during growth.

In 2008, Konstantin V. Emtsev et al. made significant advancements in enhancing the uniformity and quality of epitaxial graphene. They achieved this by subjecting silicon carbide substrates to a high-temperature Ar atmosphere within a closed space flushed with inert gas Ar or other high-temperature resistant materials, in contrast to ultra-high vacuum environments. Continuing their research trajectory, in 2009, Konstantin V. Emtsev et al. conducted annealing of 6H-SiC (0001) in Ar (p=900mbar, T=1650 ℃, t=15min), achieving a nominal thickness of 1.2ML. Building on these findings, in 2012, Hertel et al. cultivated higher-quality graphene by thermally decomposing silicon carbide substrates at 1650 ℃ under an argon gas flow at near-ambient pressure.

The genesis of graphene emerges from the evaporation of silicon atoms from the substrate. At a given temperature, the presence of high-pressure argon gas curtails the rate of silicon evaporation. This phenomenon occurs because silicon atoms desorbed from the surface possess a finite likelihood of being reflected back to the surface through collisions with argon atoms, a concept initially elucidated by Langmuir. Indeed, in the presence of an Ar atmosphere, no silicon sublimation from the surface was observed, even at temperatures as elevated as 1500 ℃, whereas silicon desorption commences at 1150 ℃ under vacuum conditions. Consequently, the attainment of significantly higher growth temperatures leads to augmented surface diffusion, facilitating surface reconstruction prior to graphene formation. This, in turn, culminates in a notable enhancement in surface morphology. Macroscopic step structures also play a role in enforcing stricter thickness control. New graphene layers originate from step edges; therefore, having fewer steps along well-defined crystalline directions diminishes the nucleation density of multilayer graphene. The mobility achieved from Ar annealing is approximately twice as high at 300 K and roughly three times as high at 27 K compared to graphene grown under vacuum conditions. This disparity underscores the substantial negative influence of abundant domain boundaries in vacuum-grown graphene on carrier mobility. Conversely, no significant disparity in electron mobility is observed between the two geometries, indicating a minor role of step edges, akin to graphene field-effect transistors in multilayer graphene. Throughout processing, numerous step bunching events occurred, yielding parallel terrace arrays with widths of up to 3 μm and lengths surpassing 50 μm.

Annealing in an argon atmosphere unveils expansive, uninterrupted terraces that extend longitudinally parallel to the step edges, with step bunching yielding macroscopic terraces spanning 5-8 times the width of the original ones. These macroscopic steps align with the original ones, their height proportionally increased by a similar factor, averaging 8-15 nm. Notably, the domain size of monolayer graphene exceeds that of samples annealed under vacuum. Initiation of the new graphene layer occurs at the step edges of the substrate surface, presenting a well-ordered alignment relative to the substrate. This alignment permits the graphene and SiC basal unit vectors to orient at a 30 ° angle to the substrate step direction, with step width determined by the surface orientation discrepancy relative to the primary crystalline direction and azimuthal orientation. In sharp contrast to the inferior quality formation observed in vacuum graphitization, films grown under argon exhibit markedly enhanced surface morphology.

In 2013, Tao Peng et al. endeavored to alleviate the demanding requirements of high synthesis temperature and ultra-high vacuum (UHV) conditions by employing defect-rich, long-range disordered amorphous carbonaceous precursors. Operating at a relatively modest temperature of 800 ℃ and atmospheric pressure, they initiated reactions with gases such as Cl_2 on the substrate. Through chlorination, they achieved direct conversion of amorphous SiC ($a-Si_{12-x}\,C_x$) nanoshells (nanofilms) into graphene within a one-hour exposure to a chlorine (Cl2) atmosphere. The selection of this method stemmed from the isotropic nature of $a-Si_{12-x}\,C_x$, its cost-effectiveness, and its versatility in synthesis. Subsequent to preparation, graphene was detached from the silicon carbide substrate using Electrochemical Delamination (ECE) techniques with a voltage application of 0.98 V. Carbon atoms underwent continuous consumption via Cl_2 reaction, resulting in defect formation, thereby reducing the energy barrier for the transition from amorphous carbon to graphene. Cl_2 interaction with Si atoms within the $a-Si_{12-x}\,C_x$ nanoshell led to the formation of a thick, highly defective carbon-rich layer, which subsequently transformed into thermally stable few-layer graphene. Notably, graphene's impermeability to gases prevents further etching of SiC by Cl_2, leaving behind a b-SiC core once a continuous graphene layer is established.

In a controlled environment within a sealed sample chamber, graphene is synthesized utilizing the innovative Face-to-Face epitaxial graphene technique, which effectively mitigates the sublimation of silicon (Si) and regulates the growth of graphene. This technique, termed CCS epitaxial graphene growth, stands out for its simplicity, as it requires no specialized structural configurations, making it accessible, cost-effective, and reusable. By employing two SiC substrates arranged in a stacked configuration, precise control over the partial pressure of Si is achieved, facilitating the production of high-quality C-face epitaxial graphene. Operating at elevated temperatures of approximately 1600 ℃, the space between the stacked SiC substrates acts as a barrier, effectively reducing the rate of Si atom desorption from the SiC substrate surface. This setup creates a localized environment with a relatively high Si partial pressure at the substrate surface. Consequently, the heightened Si partial pressure near the surface curtails the rapid consumption of Si on the SiC surface, thereby decelerating the graphene growth rate. This controlled process extends the timeframe for the deliberate growth of epitaxial graphene at the same temperature, ultimately yielding epitaxial graphene of superior quality.

2.2 Si and C terminal surface

The epitaxial growth of graphene exhibits distinct rotation angles between the Si face and C face of SiC substrates. While a fixed rotation angle characterizes the relationship between Si-face epitaxial graphene and SiC crystals, the rotation angle between C-face epitaxial graphene and SiC demonstrates greater variability. This discrepancy stems from the asymmetric characteristics of the Si and C terminations present on single-crystal SiC substrates. Consequently, the structural evolution, growth pathways, and reconstruction mechanisms differ significantly between these two terminations. As a result, the fabrication processes and the structural and property characteristics of epitaxial graphene display notable variations based on the termination type. For instance, the temperature required for graphene preparation on the C face is approximately 150 ℃ lower than that on the Si face. Epitaxial graphene grown on the Si face tends to have fewer layers and lower carrier mobility, typically reaching up to 20,000 $cm2\cdot V^{-1}\cdot s^{-1}$ or higher. Conversely, graphene grown on the C face exhibits characteristics akin to turbostratic multilayer graphene, featuring more layers yet displaying properties similar to mechanically exfoliated monolayer graphene, with carrier mobility reaching up to 250,000 $cm2\cdot V^{-1}\cdot s^{-1}$. Research indicates that these differences in electrical properties primarily arise from variations in terminations and the transition layers interfacing between the terminations and the substrate.

Controlling the growth of graphene on the C face of SiC substrates presents challenges in both ultra-high vacuum (UHV) and Ar atmospheres. In UHV conditions, the monocrystalline domain size of SiC C-face epitaxial graphene remains relatively small, typically a few hundred nanometers. While high-quality graphene with larger domains can be achieved in an Ar atmosphere, the process requires substantially higher preparation temperatures. Additionally, the fabrication of graphene-based devices necessitates the precise growth of high-quality epitaxial graphene. Therefore, achieving controlled graphene growth is paramount for the manufacturing of graphene-based devices, emphasizing the importance of refining growth techniques and understanding the underlying mechanisms governing graphene growth on the C face of SiC substrates.

J. Hass et al. employed 4H-SiC substrates to synthesize graphene via high-temperature treatment in ultra-high vacuum environments, targeting both the C-terminated and Si-terminated surfaces. Graphene fabrication involved heating the C-terminated surface to 1430 ℃ for 5-8 minutes, yielding approximately 7 layers, while the Si-terminated surface required heating to temperatures ranging from 1400 ℃ to 1440 ℃ for 6-12 minutes, resulting in 2-3 layers of graphene. Surface morphology analysis was conducted using X-ray and LEED tests, revealing a correlation between enhanced sample structural order and recent magnetotransport measurements. Subsequent hydrogen etching unveiled the wider step width of the C-terminated surface compared to the Si-terminated surface (approximately 1.4μm versus 0.2μm on average), leading to significantly larger average structural magnetic domain sizes on C-face graphene. Furthermore, graphene growth occurred at lower temperatures on the C-terminated surface compared to the Si-terminated surface, where achieving four to five layers of graphene on Si necessitated temperatures exceeding 1500 ℃. In contrast to graphene produced on Si-terminated surfaces as documented previously, the inherent substrate roughness stemming from C-termination sublimation was notably suppressed, resulting in a tenfold increase in the electron mobility of graphene films prepared on the C-face of SiC, with coherence lengths surpassing 1μm.

In epitaxial graphene grown on 4H-SiC (0001), the phenomenon of Hall resistance quantization, commonly observed in exfoliated graphene, has not been detected. This discrepancy can be attributed to several key factors inherent to the epitaxial growth process on this substrate. One primary challenge is the difficulty in achieving precise atomic-scale thickness control during film growth, particularly on the C-terminated surface. This leads to the formation of graphene films with multiple layers, which lack the uniformity typically found in exfoliated graphene sheets. Additionally, there are notable variations in carrier density (or doping levels) among the layers grown on the Si-terminated surface, further complicating the electronic properties and transport phenomena. These challenges highlight the complexities associated with epitaxial graphene growth on 4H-SiC (0001) and underscore the importance of optimizing growth conditions to achieve desired electronic properties for future device applications .

3. Summary and outlook

In ultra-high vacuum (UHV) environments, the synthesis of graphene involves the thermal decomposition of SiC substrates. Despite the relatively low temperatures required for graphene production (around 1200 ℃), achieving this process demands exceedingly high vacuum conditions, typically maintained at pressures of 10^-8 Torr. Within such vacuum environments, silicon (Si) desorption proceeds rapidly. During the temperature range conducive to graphene formation, defects, scratches, and other nucleation sites on the substrate facilitate the rapid growth of graphene. Conversely, regions with superior substrate surface quality exhibit minimal or negligible graphene formation, often resulting in either sparse graphene layers or none at all. Consequently, the quality and thickness of graphene synthesized in UHV environments tend to be inconsistent. While substrate pretreatment can somewhat encourage the formation of uniform nucleation points on the substrate surface, it does not significantly improve the overall quality of epitaxial materials.

To mitigate the limitations associated with graphene synthesis through thermal decomposition in ultra-high vacuum (UHV) settings, researchers have turned to producing epitaxial graphene on SiC in inert gas atmospheres. Conducting the process at atmospheric pressure and elevated temperatures plays a crucial role in decreasing the rate of silicon (Si) atom desorption, leading to a more uniform deposition of Si atoms on the substrate surface during the growth phase. Consequently, this approach yields epitaxial graphene of superior quality. Nonetheless, it necessitates exceedingly high graphitization temperatures and meticulous regulation of gas flow rates, thus elevating both the complexity of the procedure and associated costs. Graphene can be prepared by reacting chlorine gas with silicon carbide, a method with relatively low environmental requirements. However, it necessitates initial substrate treatment, yields significant by-products, and presents challenges in controlling reactions on the substrate, potentially leading to substrate contamination. These factors limit the application of the primary product in the field of microelectronics.

High-quality epitaxial graphene is achieved through the capping method, a technique designed to regulate the rate of silicon atom desorption from the SiC surface. This method employs a specialized graphene enclosure structure, which effectively slows down desorption, even under minimal or no protective gas conditions. Through the capping method, researchers can consistently produce high-quality epitaxial graphene on SiC substrates, with the flexibility to control the number of graphene layers and single crystal domain sizes by adjusting process parameters. However, while the capping method operates at lower temperatures, further investigation is warranted to elucidate the nature of generated by-products and refine reaction conditions for optimal outcomes.

In the realm of graphene synthesis via silicon carbide decomposition, the prevailing methods demand stringent experimental conditions, ranging from high vacuum and low temperature to high temperature and low vacuum. The crux of successful synthesis lies in impeding the rupture of Si-C bonds, promoting the formation of C-C bonds, and ensuring uniform defect distribution, crucial for nucleation points. The introduction of inert gases effectively alleviates vacuum demands, facilitating silicon carbide preparation under reduced vacuum and temperature settings. Moreover, the implementation of spatially enclosed structures enhances graphene quality, presenting a promising avenue for optimization in synthesis methodologies.

Henceforth, in the development of epitaxial graphene on silicon carbide, the convergence of diverse methodologies holds promise for achieving uniform, high-quality, large-area, and controllable-layer graphene. By integrating the benefits of inert gases and employing enclosed structures within low vacuum and low temperature environments, exemplified by the capping method, the pace of silicon sublimation can be moderated, ensuring the uniform dispersion of nucleation sites while concurrently mitigating process demands.

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