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Research on RF Voltage Measurement Method of Chip Pins

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Abstract: *As the core device of electronic equipment, integrated circuit (IC) usually produces large high-frequency electromagnetic interference. In order to study the generation mechanism and suppression methods of such noise, accurate noise measurement and extraction must be carried out. At present, the measurement standard of chip level electromagnetic compatibility is not perfect, and the high-frequency characteristics of pin noise are difficult to be measured accurately. In order to achieve accurate chip pin RF voltage measurement, this paper designs a chip pin RF voltage measurement method, establishes the 3D model of the chip pin RF voltage measurement module, studies the effects of its wiring, via, substrate dielectric constant and other parameters on its high-frequency signal transmission performance, and then optimizes the module. Simulation and experimental results show that the optimization method effectively improves its high-frequency signal transmission characteristics. Finally, the RF voltage of the output pin of the active crystal oscillator is extracted by using the detection system designed in this paper.*

Keywords: *Electromagnetic compatibility, RF voltage, Impedance matching network, Insertion loss*

1. Introduction

With the rapid development of communication technology and the continuous progress of integrated circuit technology, all kinds of electronic equipment pour into the market, with smaller and smaller volume, higher and higher accuracy requirements, and the working frequency gradually develops to the RF section [1]. As the core unit of electronic information system, the increase of IC density is accompanied by more and stronger electromagnetic interference [2]. In the general environment, the electromagnetic field level of the surrounding space is also gradually improved. When electronic equipment or systems work in such a complex environment, they have to evaluate their electromagnetic compatibility [3].

At this stage, according to the types of electronic equipment, it is mainly divided into industrial, commercial, civil and military categories, and relevant mandatory electromagnetic compatibility testing standards are formulated, such as CCC certification of civil and commercial electronic products. However, the measurement of EMC of these electronic equipment is often limited to the measurement of the whole equipment, and there is still a lack of EMC measurement standards for integrated circuit component level. With the improvement of integrated circuit integration, more and more components are integrated into the chip, and a single chip contains a complete system. High integration, complex circuit, and the rapid change of current and voltage inside the chip will produce electromagnetic emission (EME), which will affect the waveform and working characteristics of external output current and voltage of the integrated circuit, which has brought unprecedented challenges to the chip testing work [4-6]. Therefore, the design of chip detection circuit with high performance and high reliability is of great significance.

In high frequency and microwave circuits, the problem caused by impedance mismatch is particularly obvious. The energy transmitted by the circuit will be reflected back to produce standing wave, which will cause the damage of the insulation layer of the feeder and the final power amplifier tube of the transmitter [7]. Therefore, it is necessary to design an impedance matching network between the power supply end and the load end to convert the impedance of the load end into an impedance form matching the impedance of the power supply end [8-9]. Impedance matching network can transmit all high-frequency microwave signals to the load point, avoid complex circuit problems such as interference and reflection, and almost no signal will be reflected back to the source point, which greatly improves energy efficiency. Therefore, the design of impedance matching network with good performance is of great significance to the RF voltage measurement module of chip pin.

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Referring to the relevant requirements and detection methods of the international standard IEC 61967-4 discussion draft, this paper designs a pin RF voltage detection system based on impedance matching network and spectrum analysis module. With the joint simulation of ADS software and cadence software, the loss of PCB is simulated and analyzed, and the circuit is optimized according to the simulation results to ensure the continuity of the optimized circuit board impedance and small insertion loss [10].The practical application shows that the impedance matching network has good performance and strong practicability.

2. Development of RF voltage detection system

2.1 Principle of RF voltage detection

The rapid voltage and current changes of parasitic components inside the IC and MOS tubes inside the chip produce electromagnetic interference, which excites RF current and RF voltage at the IC pin. The conductive current between the RF and the EMI pin on the PCB forms a circuit. These loops can be regarded as transmitting loop antennas. Compared with the size of these circuits, the circuit of IC internal structure is smaller. The noise generated by IC is mainly caused by the high-frequency current generated during its operation, and its spectrum component is very rich. For the measurement and evaluation of these noise sources, we can use RF voltage measurement.

Because the switching frequency of each type of MOS tube is different, the amplitude and frequency of RF voltage and current are different, so each RF current has a different release circuit. Figure 1 shows three circuits of RF signal propagation. Circuit 1 is the power supply line of IC, circuit 2 is the signal output path, and circuit 3 is the circuit composed of signal output port and IC ground [11].

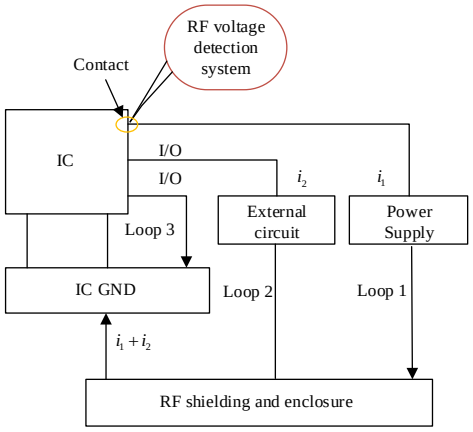

Figure 1: Schematic diagram of electromagnetic interference circuit of IC port

When the chip works, the application scenarios are different, such as PCB wiring with a connection length greater than 10cm or the pins of the tested IC under constraints. In order to study the conducted electromagnetic interference of a pin to the tested IC, the RF voltage is measured by the voltage probe. These pins are terminated with a typical antenna impedance of 150 Ω. The input terminal of the voltage probe is a pin of the chip, and the measurement results are displayed by the external spectrum analyzer or EMI receiver. The input resistance of spectrometer and receiver is generally 50 Ω, so it is necessary to connect 150 / 50 Ω impedance matching network as load. This method is RF voltage measurement.

2.2 Test system

The RF voltage detection system of this design is shown in Figure 2. The system includes test chip circuit board, voltage probe, impedance matching network and EMI receiver. The left side is the test chip. The voltage probe is composed of probe adjustment seat, tungsten steel probe and probe sleeve. The probe can be used 45 °or vertically, as shown in Figure 3. The effective frequency range of tungsten steel probe is 0-3GHz; The effective frequency range of impedance matching network is 150khz-1ghz. After optimization, the insertion loss in 50 Ω system reaches 11.8db, which meets the standard requirements; The output end of the voltage probe is connected to the EMI receiver to measure the RF voltage of the output pin when the chip works normally.

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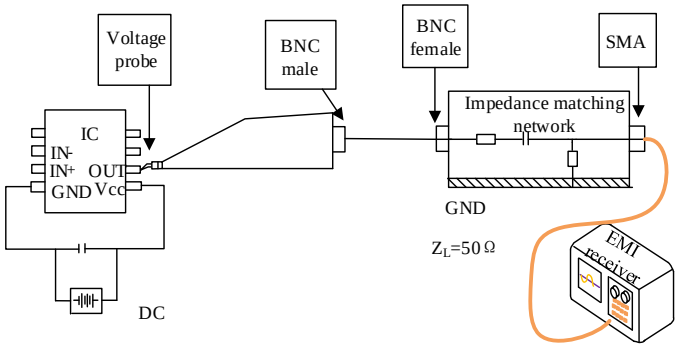

Figure 2: RF voltage test system

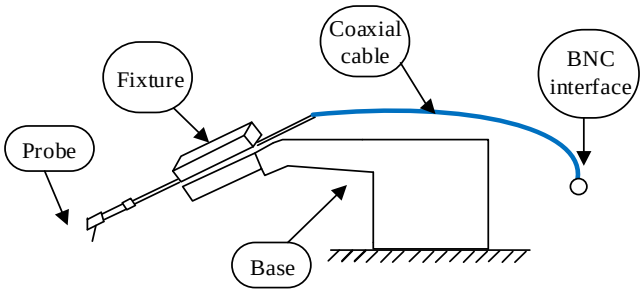

Figure 3: Design drawing of voltage probe

3.3 Figure 4 impedance matching network

Impedance matching refers to the mutual adaptation of the characteristic impedance of the excitation source or transmission line and the load impedance. After the impedance matching is realized, the output power of the integrated circuit reaches the maximum. At this time, the signal will not be reflected and the energy will be absorbed by the load. When the load impedance does not meet the conjugate matching condition, the impedance matching network can convert the load impedance into the conjugate of the excitation source impedance, so as to realize impedance matching.

According to IEC 61967-4, in most cases, the cable network can be represented by a 150 Ω impedance antenna. In order to obtain accurate measurement results in the frequency range of 150kHz ~ 1GHz, a terminal network of 150Ω±20Ω shall be used. Generally, the input impedance of the measuring equipment is 50 Ω, so the impedance matching network should be able to match the signal line impedance and the equipment impedance. The impedance matching network is shown in Figure 4.

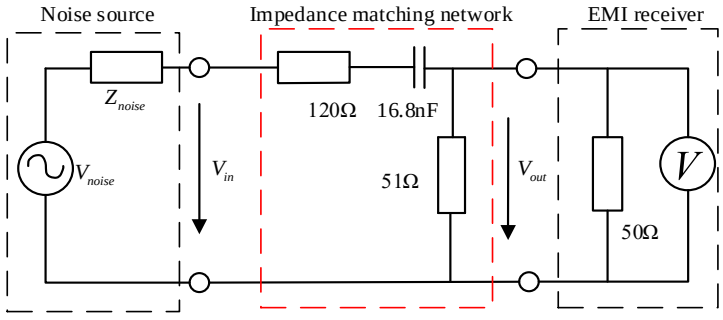

Figure 4: Impedance matching network

The impedance matching network characteristics include the input impedance Zi of the 50 Ω terminal, the insertion loss S_{21} in the 50 Ω system, and the voltage ratio V_{out} / V_{in}. The selection of capacitance value is the difficulty. Each characteristic value within the frequency range can be calculated by MATLAB, and the final capacitance value is 16.8nf.

Formula (1) is the input impedance calculation method of 50 Ω terminal，Z_i, R_1 and R_2 are the internal resistance of impedance matching network, C1 is the selected capacitance, and RMI is the internal impedance of receiver. The simulation results are shown in Figure 5, which can meet 145 ± 20 Ω.

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$$Z_i = \left| R_1 + \frac{1}{\mathrm{j}wC_1} + \frac{R_2 \times R_{mi}}{R_2 + R_{mi}} \right| \tag{1}$$

Formula (2) is the insertion loss in a 50 Ω system. The simulation results are shown in Figure 6, which can meet -11.75 ±2dB.

$$\begin{aligned} IL_{50} &= 20\log_{10}\left| \frac{\frac{R_2 \times R_{mi}}{(R_2 + R_{mi})(Z_i + 50)}}{\frac{R_{mi}}{R_{mi} + 50}} \right| \\ &= 20\log_{10}\left| \frac{R_2 \times R_{mi}}{(R_2 + R_{mi})(Z_i + 50)} \frac{R_{mi} + 50}{R_{mi}} \right| \end{aligned} \tag{2}$$

Formula (3) is the calculation formula of voltage ratio. The simulation results are shown in Figure 7, which can meet - 15.2 ±2dB.

$$VR = 20\log_{10}\left| \frac{R_2 \times R_{mi}}{(R_2 + R_{mi})Z_i} \right| \tag{3}$$

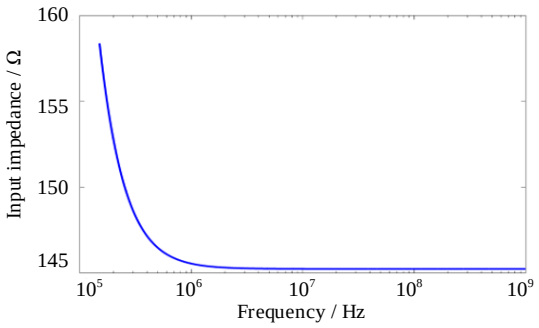

Figure 5: Input impedance of 50 Ω terminal

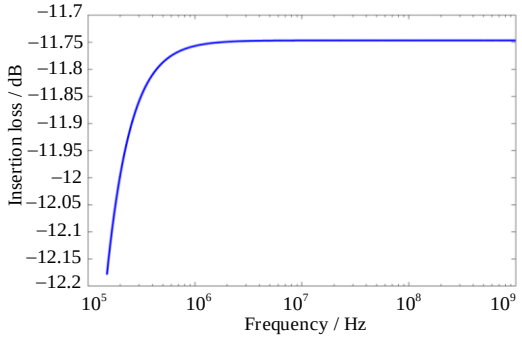

Figure 6: Insertion loss in 50 Ω system

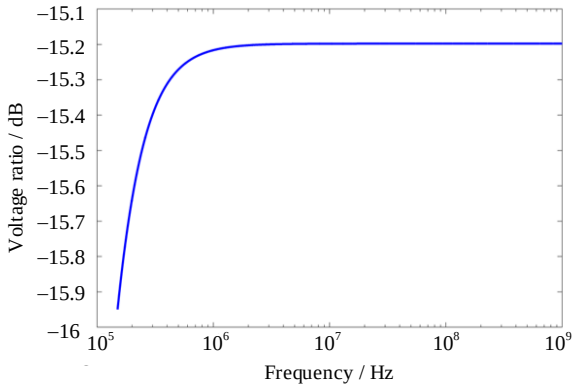

Figure 7: Voltage ratio V_{out} / V_{in}

3. Signal Integrity simulation and optimization of PCB

3.1 PCB board modeling

Based on the impedance matching network theory, the PCB model is established, as shown in Figure 8. The approximate size of the model is 6cm × 2 cm × 0.3 cm, PCB is a 4-layer structure, in which the metal layer is Cu, and the electrical parameters are σ= 5. 8 × 107 S/m， The material of the dielectric layer is FR4, and the parameters of each layer are shown in Table 1.

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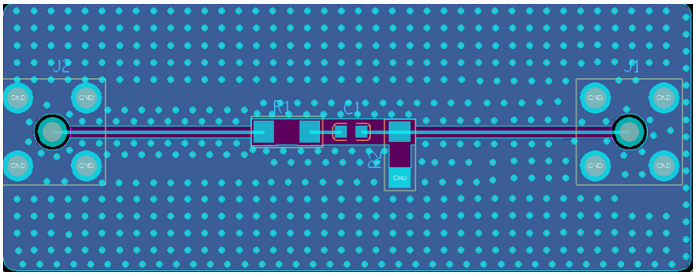

Figure 8: Impedance matching network PCB board

Table 1: Stacking parameters

Layer Name	Type	Material	Thickness/mil
SOLDER_MASK_TOP	Dielectric	Fr4	1
TOP	Signal	Copper	1.78
DIELECTRIC_0	Dielectric	Fr4	47.24
BOTTOM	Signal	Copper	1.78
SOLDER_MASK_BOTTOM	Dielectric	Fr4	1

3.2 Simulation and optimization

Insertion loss refers to the signal loss between the transmitter and the receiver after inserting into the network. By optimizing the insertion loss value, the accuracy of RF voltage test in high frequency part can be improved. Using ADS software, import PCB board and carry out S-parameter simulation. Combined with the influence of PCB wiring, ground hole and copper coating on the loss, the impedance matching network is qualitatively analyzed to provide guidance for the development of detection circuit.

3.2.1 Influence of PCB routing

In the design of high-speed PCB board, the routing and width of signal line will have an impact on the insertion loss. This design studies the linewidth. The control variable method is used to select the diameter of 10 mil and the number of 30 vias. The insertion loss is extracted by changing the linewidth. Figure 9 shows the insertion loss of impedance matching network when the linewidth is set at 5MIL, 9MIL, 13mil and 17mil.

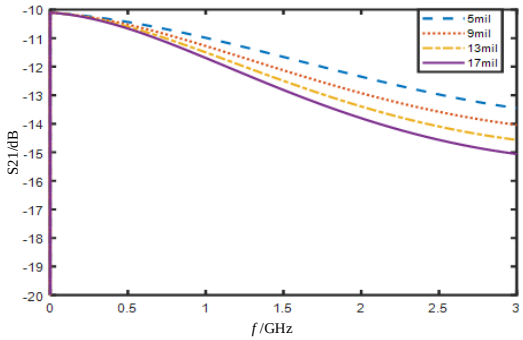

Figure 9: Effect of linewidth on insertion loss

The simulation results show that the insertion loss before 0.5ghz is almost the same, and after 0.5ghz, the insertion loss increases with the increase of linewidth. The smaller the insertion loss, the better the signal integrity, but the linewidth cannot be infinitely reduced. After consulting the plate making process data, confirm the linewidth as 6mil.

3.2.2 Influence of PCB via

PCB vias can be divided into signal vias and power / ground vias. The ground vias are mainly used for heat dissipation and connecting the layers of multi-layer boards. From the perspective of EMI, the high-speed signal area needs more ground holes, which can improve the overall anti-interference ability

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of the board and reduce the insertion loss of the system. However, the unreasonable placement of ground holes in the analog signal area will become an interference source, and more ground holes will also affect the impedance and integrity of the high-speed line. In this design, 12mil grounding holes are added around the signal line and signal vias. Using the control variable method, only the number of ground holes is changed, and the number of vias is 0, 3, 15 and 30 respectively. The insertion loss results are shown in Figure 10.

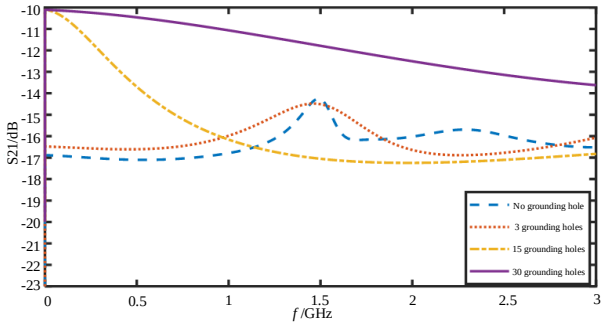

Figure 10: Effect of the number of ground holes on insertion loss

The simulation results show that at 1GHz frequency point, the loss of 30 ground holes is reduced by about 3dB than that of no ground holes. Due to the limited area of PCB, the number of ground holes cannot be increased without an upper limit, and when the number of local holes is greater than 30, the insertion loss in 1GHz changes little. After consulting the plate making process data, this design adopts the design scheme of 0.5mm from the signal line and signal through holes, 1mm through hole spacing and 30 quantity.

3.2.3 Effect of substrate dielectric constant

After the PCB board component layout is completed, the board area needs to be filled with copper. If there are too many zero potential points on the board, select the reference "ground" to cover copper independently. The significance of copper coating mainly has three points: reducing the ground wire impedance, facilitating the current flow and improving the anti-interference ability of the equipment; Reduce voltage drop and improve power supply efficiency; The copper area is connected with the ground to reduce the loop area and conductive interference. Using the control variable method, set the line width of 6mil, the via diameter of 10mil and the number of 30. The simulation results are shown in Figure 11.

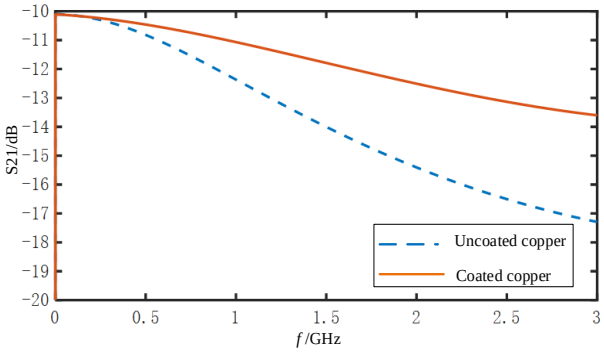

Figure 11: Effect of copper cladding on insertion loss

Obviously, whether copper coating directly affects the insertion loss value. When the frequency is greater than 0.5ghz, the difference between the insertion loss of the two increases gradually. When the frequency reaches 1GHz, the insertion loss value of the non copper clad laminate becomes - 13dB, and the higher the frequency, the greater the difference, which exceeds the characteristics of the impedance matching network. Therefore, this design adopts PCB board with copper coating on the surface.

3.3 Analysis of optimization results

Connect the impedance matching network test board as shown in Figure 12, test the insertion loss of the PCB board made by VNA, and compare and analyze with the simulation results. The results are

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shown in Figure 13.

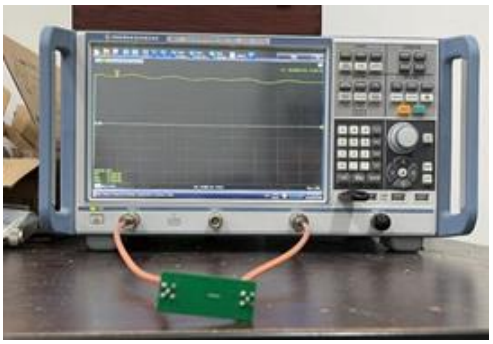

Figure 12: Insertion loss test

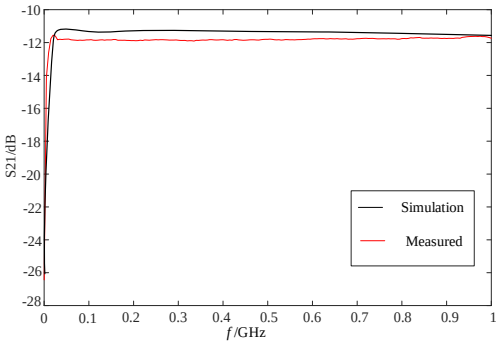

Figure 13: Comparison of simulation and measurement

Table 2: Spectrum results of simulation test

Number	Frequency (MHz)	Simulation value (dB)	Measured value (dB)	Difference (dB)
1	400	-10.66	-11.43	0.77
2	600	-10.88	-11.46	0.58
3	800	-11.25	-11.62	0.37
4	1000	-11.66	-11.88	0.22

It can be seen from Figure 13 and table 2 that after 150kHz, the difference between the simulated and actual insertion loss values is about 0.5dB. The reason may be caused by welding process or external environment, but it is still within the characteristic range of impedance matching network, which proves the effectiveness of the designed impedance matching network and can meet the requirements of RF voltage detection.

4. Application of RF voltage detection system

4.1 Hardware circuit construction

Crystal oscillator is one of the most commonly used electronic components in electronic circuits. Crystal oscillator uses a crystal that can convert electrical energy and mechanical energy into each other. Working in resonance state, it can provide stable and accurate single frequency oscillation.

Generally, pin 1 of the four pins active crystal oscillator is an empty pin. In counterclockwise order, pin 2 is the grounding pin, pin 3 is the output pin and pin 4 is the power input pin. This section takes the four pin active crystal oscillator as an example to build a simple working circuit. The schematic diagram and the real object are shown in figures 14 and 15 respectively.

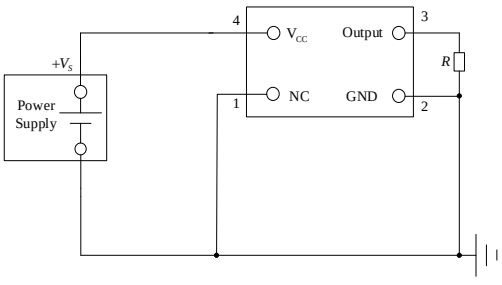

Figure 14: Circuit schematic diagram

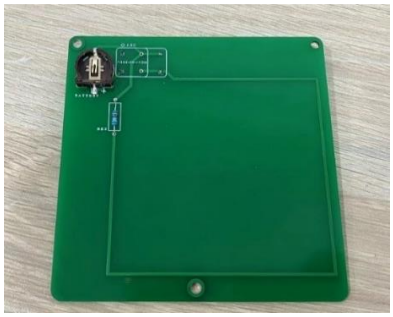

Figure 15: Hardware circuit

4.2 RF voltage test

The RF voltage detection system of FIG. 16 includes a voltage probe, an impedance matching network and an EMI receiver. The probe, matching resistance test board, impedance matching network and connecting device are self-made equipment. After VNA test, the insertion loss meets the standard requirements and has good performance. The noise voltage of output pin 3 measured by the voltage probe is shown in Figure 17.

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Figure 16: RF voltage test

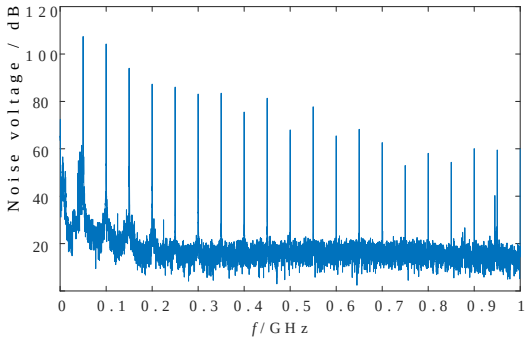

Figure 17: RF voltage test results of No. 3 output pin

It can be seen from the measurement results that the maximum RF voltage of the crystal oscillator output pin is close to 110dbuv, and shows a gradual decreasing trend with the increase of frequency.

5. Conclusion

In this paper, the RF voltage measurement method of chip pin is studied, and a detection system which can accurately measure the RF voltage of chip pin is designed.利 Using ADS simulation software, the effects of wiring, via, substrate dielectric constant and other parameters on high-frequency signal transmission performance are studied, the PCB layout is optimized, and the insertion loss is tested by vector network analyzer to verify the accuracy of RF voltage measurement module. Design the active crystal oscillator working circuit, measure the RF voltage of the crystal oscillator output pin, and verify the effectiveness of the designed RF voltage detection system.

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