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Optimization model design of multi-factor nonlinear ring oscillator

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Abstract: *Ring oscillator is an important structure of digital chip, and the optimized design of ring oscillator becomes especially important with the booming development of chip manufacturing industry. In this paper, a ring oscillator power consumption optimization model and a multi-project wafer circuit installation model are constructed to provide an effective theoretical optimization model support for the actual production life of digital chips. Under the premise of ensuring the minimum overall power consumption, the total power consumption of the ring oscillator is used as the objective function, and the particle swarm optimization algorithm is used to solve the number of inverters of the oscillator and the Length of the transistor is 213nm and the minimum total power consumption of the ring oscillator is 0.8 mW. Moreover, the jigsaw puzzle idea is used as the circuit design concept, and the maximum area of the seventh chip is obtained after the reasonable placement of six fixed area chips 0.554mm×1.774mm.*

Keywords: *Ring oscillator design; Oscillator performance optimization; particle swarm optimization algorithm*

1. Introduction

As the core of modern intelligent technology, the research value of the chip is climbing, and its powerful functions are mainly realized by integrated circuit technology. As an important building block of semiconductor technology [1,2], oscillators can be widely used in integrated circuits and microelectronic processors, making it possible to make electronic products multifunctional and portable. Common oscillators include LC oscillators, CMOS oscillators, crystal oscillators and ring oscillators, among which, the ring oscillator is a ring circuit with multiple identical inverter units connected in series, which has the advantages of low power consumption and easy integration [3] and has a wide range of applications in real life.

The purpose of this paper is to optimize the design of a ring oscillator made by combining PMOS tube and NMOS tube-based inverter as the basic unit, taking into account the operation speed, area and power consumption of the chip.

To design a ring oscillator with an output frequency of 5MHz, it is required to solve for the number of inverters of the oscillator and the size of Length and Width of the transistors, while keeping the overall power consumption to a minimum.

The seven chips (six of which have known areas) are mounted on the same wafer of known size, and the appropriate size of each ring oscillator is required to be designed so that the number of oscillators mounted on the seventh chip is as large as possible, while ensuring that the output power of each ring oscillator is 2MHz and the overall power consumption is as small as possible.

2. Assumptions

In this paper use the following assumptions.

1) The operating phase of the inverter can be divided into linear phase and saturation current phase, and because the linear phase of the inverter is very short, the current usually enters the stable operating state and then keeps the saturation current for operation. Therefore, it is assumed that the currents during the output power calculation are saturated flow, and the influence of the currents in the linear region on

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the results is not considered.

2) Assume that the area of the ring oscillator is the sum of the areas of the inverters it contains, without considering the area of the connecting lines, according to the ring oscillator version given in the Appendix.

3. Model construction and solving

3.1 Power consumption optimization model

In this part, it is necessary to solve the optimal size parameters with the minimum power consumption of the oscillator, considering the three factors of operation rate, area, and power, with power as the most dominant factor. For this purpose, it is first necessary to determine the expression of power consumption, and it is known from the review of data that the power consumption of the inverter is divided into two categories: dynamic power consumption contains switching power consumption and short-circuit power consumption, and static power consumption contains leakage power consumption [4,5]. Therefore, the expressions for the three types of power consumption need to be analyzed before the total power consumption can be expressed. After that, the power consumption optimization model is constructed with the objective function of minimizing the total power consumption under the equation and non-equation constraints specified in the question and solved.

3.1.1 Model building

Firstly, solve for the switching power consumption of an inverter.

The power consumption of a single inverter is the power consumption due to the alternate charging and discharging of the load capacitor, independent of the area of the diode. For the power consumption due to capacitor charging, the corresponding process is that the single load capacitor CL is charged through the PMOS tube, and its voltage rises from 0 to VDD. During the charging process, its total energy taken from the power supply is partly stored in the load capacitor CL and partly consumed in the PMOS device. Assuming that the NMOS and PMOS devices do not conduct at the same time, the equivalent circuit in Figure 1 can be used to represent this.

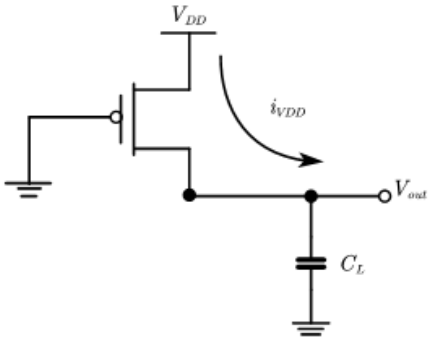

Figure 1: Equivalent circuit diagram of load capacitor charging

The dynamic power consumption due to capacitor discharge is caused by the discharge of the capacitor during the flip from high to low level, and the energy stored in the capacitor is consumed in the NMOS tube.

To calculate the power consumption, the generated energy is calculated first, and the energy EC that can be stored by the capacitor CL is calculated by integrating the instantaneous power consumption over the corresponding period after the level flip is over as follows

$$E_C = \int_0^\infty i_{VDD}(t) v_{out} \mathrm{d}t = \int_0^\infty C_L \frac{\mathrm{d}v_{out}}{\mathrm{d}t} \mathrm{d}t = C_L \int_0^V v_{out} \mathrm{d}v_{out} = \frac{C_L V_{DD}^2}{2} \tag{1}$$

Observing the above equation, it is found that during the low level flip to high level, the charge of CL, and in order to meet the charge of CL, the power supply needs to supply the energy of $C_L V_{DD}^2 \left(= Q \times V_{DD} \right)$. Energy stored in the capacitor indicates that half of the energy supplied by the power supply is consumed on the PMOS tube and half is stored on CL. This energy consumption is independent of the size of the PMOS tube. During the high flip to low level, i.e., the discharge process,

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the charge on the capacitor CL is removed and the energy is consumed on the NMOS tube, and the energy consumed is also independent of the NMOS tube size.

In summary, the energy consumed is fixed for each switching cycle (consisting of flipping from low to high and from high to low). In this paper, we set the power consumed by the device as

$$P_{dn} = C_L V_{DD}^2 f_{0\to 1} \tag{2}$$

The switching activity is related to the nature and statistical properties of the input signal: if the input signal remains constant, no switching behavior occurs and the dynamic power consumption is zero; if the signal changes rapidly, it causes multiple switching and generates power consumption.

Due to the complexity of the switching activity calculation, in this paper, equation (2) is transformed into

$$P_{dmn} = C_L V_{DD}^2 f_{0\to 1} = C_L V_{DD}^2 P_{0\to 1} f = C_{EFF} V_{DD}^2 f \tag{3}$$

The expression for the maximum possible rate at which the input change event occurs is

$$f = \frac{1}{T} = \frac{2}{t_{up} + t_{\text{down}}} \tag{4}$$

Switching power consumption for the whole circuit There is

$$P_k = C V_{DD}^2 f_{0\to 1} = N C_L V_{DD}^2 f_{0\to 1} \tag{5}$$

Solving for the short-circuit power consumption of the direct path current. In the case of the actual circuit design, the assumption that the input waveform rises and fall times are zero is incorrect because the extreme cases are not considered [5]. Since the slope of the input signal is not infinite, a direct path will appear between VDD and GND during the circuit switching process for a short period of time, at which time the NMOS tube and PMOS tube conduct at the same time, and the equivalent circuit is shown in Figure 2.

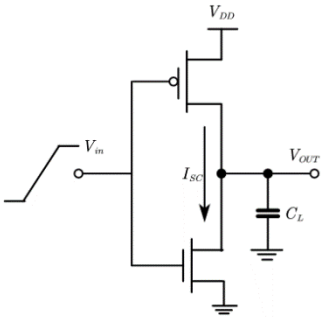

Figure 2: Short circuit process diagram

Based on the assumption of a global 50% reference value, then the power consumption generated at rising edge time in one cycle is equally divided with the power consumption generated at falling edge time. Then it can be derived that the energy consumed by the ring oscillator Edp during each switching cycle is calculated as follows.

$$E_{dp} = V_{DD} \frac{I_{peak} \cdot t_{sc}}{2} + V_{DD} \frac{I_{peak} \cdot t_{sc}}{2} = t_{sc} \cdot V_{DD} \cdot I_{peak} \tag{6}$$

Then the average power consumption of the ring oscillator in the steady-state operation is

$$P_{dp} = t_{sc} \cdot V_{DD} \cdot I_{peak} \cdot f = C_{sc} \cdot V_{DD}^2 \cdot f \tag{7}$$

For the slope of the straight line of the input signal, the following formula can be used to approximate its value.

$$t_{sc} = \frac{V_{DD} - 2V_T}{V_{DD}} t_s = \frac{V_{DD} - 2V_T}{V_{DD}} \times \frac{t_{r(f)}}{0.8} \tag{8}$$

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Step 3 Solve for the static power consumption of the circuit, i.e., the leakage power consumption. The static power consumption of a ring oscillator circuit can be expressed by the following relationship [5]

$$P_{stat}=I_{stat}V_{DD} \tag{9}$$

The drain current Istat is calculated as follows

$$I_{stat}=\frac{1}{2}g_m\left(V_{GS}-V_{TH}\right)^2 \tag{10}$$

Determine the total power consumption expression as the objective function.

The total power consumption can be calculated by summing up the switching power consumption, short circuit power consumption and leakage power consumption as follows.

$$P_{tot}=P_k+P_{dp}+P_{stat}=N\cdot C_L\cdot V_{DD}^2\cdot f_{0\to 1}+t_{sc}\cdot V_{DD}\cdot I_{peak}f+V_{DD}I_{stat} \tag{11}$$

Construct the model.

$$\min P_{\text{tot}}=NC_LV_{DD}^2f_{0\to 1}+V_{DD}I_{\text{peak}}t_sf+V_{DD}I_{\text{stat}} \tag{12}$$

$$s.t.\begin{cases} 120\text{nm}\le W_n\le 100\mu m \\ 120\text{nm}\le W_p\le 100\mu m \\ 60\text{mm}\le L\le 100\mu\text{m} \\ f=5\text{MHz}=\dfrac{1}{2Nt_{pd}} \\ t_{pd}=\dfrac{V_{DD}C_L}{\dfrac{W_p}{L}K_p\left(V_{DD}-\left|V_p\right|\right)^2}+\dfrac{W_n}{L}K_n\left(V_{DD}-\left|V_m\right|\right)^2 \\ V_p=0.398\text{V},V_m=0.42\text{V},C_L=KS_1,K=2nF/\mu m^2 \\ K_p=111.6634\mu\text{A/V},K_n=68.7134\mu\text{A/V} \end{cases} \tag{13}$$

3.1.2 Model solving

The program was written using Matlab to design a particle swarm algorithm for the constructed model to find the size parameters of the inverter and ring oscillator with minimum power consumption while the output frequency, i.e., the oscillator speed, was determined. The specific solution results are shown in Table 1 below.

Table 1: Power consumption optimization model solution results

Parameters	Results
PMOS tube gate width	25.276um
NMOS tube gate width	95.302um
Gate length of secondary tube	213nm
Supply voltage	0.580V
Number of inverters included in the ring oscillator	100
Minimum power consumption of ring oscillator	0.8mW

3.2 Establishment and solution of optimization model for chip integrated circuits

The minimum power expression is based on the construction of integrated circuits on chip 7 for the purpose of placing more ring oscillators. The specific modeling process is as follows.

Step 1 Determine the size of the ring oscillator. The ring oscillator consists of three inverters or more odd number of inverters connected first and last at the input and output to form a ring circuit. The arrangement of the inverters in the ring oscillator is analyzed and found to be in a "one" arrangement. To maximize the number of ring oscillators, the ring oscillator is considered to be composed of three

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inverters.

Step 2 Determine the objective function of the model. From the above results, the total power consumption of a single ring oscillator is expressed as follows

$$min\ P_{tot} = P_k + P_{dp} + P_{stat} \tag{14}$$

At the output frequency of 2KHz, because for the 7th chip, the ring oscillator is connected in series with each other, the total power consumption generated by the chip is the sum of the power consumption generated by each ring oscillator, as can be obtained from the circuit principle. That is, for the seventh chip power consumption P7 .

$$P_7 = N \cdot P_{tot} \tag{15}$$

Step 3 Construct the chip IC optimization model. Based on the objective function solved in step 2, the model is constructed under the constraints of equations and inequalities required in the text as follows.

$$min\ P_7 = N \cdot P_{tot}$$

$$s.t. \begin{cases} 120\text{nm} \le W_n \le 100\mu\text{m} \\ 120\text{nm} \le W_p \le 100\mu\text{m} \\ 60\text{nm} \le L \le 100\mu\text{m} \\ f = 2KHz = \dfrac{1}{2Nt_{pd}} \\ N = \left[\dfrac{S_7}{S_{\text{single}}} \right] \\ t_{pd} = \dfrac{V_{DD}C_L}{\frac{W_p}{L}K_p\left(V_{DD} - \left|V_{tp}\right|\right)^2} + \dfrac{V_{DD}C_L}{\frac{W_n}{L}K_n\left(V_{DD} - \left|V_{tm}\right|\right)^2} \\ V_{tp} = 0.398\text{V}, V_{tn} = 0.42\text{V}, C_L = KS_1, K = 2nF/\mu m^2 \\ K_p = 111.6634\mu\text{A/V}, K_n = 68.7134\mu\text{A/V} \end{cases} \tag{16}$$

A program is written in Matlab to find the optimal value of the objective function based on the particle swarm algorithm. Finally, the number of ring oscillators is obtained in the case of minimum total power consumption of chip 7. The relevant parameters and results are shown in Table 2 below

Table 2: Multi-Project Wafer Circuit Mounting Model Solving Results

Parameters	Results
PMOS tube gate width	61.390um
NMOS tube gate width	94.915um
Gate length of secondary tube	60.035nm
Supply voltage	1.13V
Number of inverters in a single ring oscillator	3
Minimum power consumption of a single ring oscillator	0.0065mW
Minimum power consumption of chip 7	0.685mW
Number of inverters in chip 7	14280
Number of ring oscillators in chip 7	4760

All three inverter size parameters are within the range specified in the topic and the results are reasonable. Compared with the results of Model 3, the total power consumption of this part of the oscillator has been significantly reduced. The reason is that the number of inverters included in each ring oscillator is the minimum standard value of three, so the smaller the number of inverters, the less delay time for signal flipping, and the power consumption generated by the current is reduced accordingly. It can be concluded that the optimal design of the IC is to install 4760 ring oscillators with a minimum power consumption of 0.685 mW under the premise that the power consumption generated by the chip is minimized.

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4. Conclusion

This paper discusses the energy saving problem in the process of chip fabrication from the power consumption of ring oscillator, takes the basic unit inverter as the research object, solves the optimal power consumption model of oscillator, and finally gets the most effective ring oscillator configuration scheme on the basis of ensuring the reasonable chip size. It is found that the smaller the number of inverters is, the better it is to reduce the power consumption generated when the ring oscillator works, and at the same time, it is beneficial to reduce the size of the ring oscillator, increase the number of oscillators installed in the chip, and improve the chip efficiency. In future research, this paper will focus on optimizing the chip performance while achieving reduced power consumption and improving the chip's environmental protection level.

References

[1] Zhu Mingwang. Research and design of low-voltage low-power CMOS oscillator [D]. Xiangtan University, 2019.
[2] Fei-Long Yu. An extremely low-power digitally tunable DLS ring oscillator design [D]. Anhui University, 2020.
[3] Wang D.X., Sun Y. An improved CMOS ring oscillator with frequency stabilization [J]. Microelectronics, 1999(05): 67-70.
[4] Clara_ D. Transmission delay of CMOS inverters [EB/OL]. (2021-10-16) [2022-08-07].
[5] LaBelle. Digital Integrated Circuits - Circuits, Systems and Design (2nd Edition) [M]. Beijing: Electronic Industry Press, 2010:155-165.