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Bridging Theory and Practice in CMOS Receiver Frontend Design: A Comprehensive Approach for Postgraduate Education

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Abstract: *This paper presents the integration of theory and practice in the course "CMOS Radio Frequency Integrated Circuits," underscoring the importance of both theoretical knowledge and practical software applications. The simulation practice of RF circuits is highlighted as a fusion with students' theoretical understanding. The teaching methodology utilizing Cadence Virtuoso software aims to maximize students' engagement and enthusiasm for learning and troubleshooting. Taking a receiver frontend as an example, the study models the systematic circuit design and simulation process, enabling students to acquire a comprehensive understanding of RF receiver design. This approach not only lays a solid foundation for future studies but also seeks to improve students' capability by linking theory to practice. Ultimately, the quality of education in " CMOS RF Integrated Circuits," targeting postgraduate students, is promoted progressively and effectively.*

Keywords: *CMOS RF Integrated Circuit, Practical Teaching, Receiver Frontend, Simulation*

1. Introduction

Integrated circuit design is a rapidly evolving engineering discipline featuring specialization and interdisciplinary integration, eloquently driving intelligence and digitalization progress in China. RF integrated circuits are crucial for wireless communication, radar, and the internet of things, supporting the information industry's exponential growth in the soaring commercial market[1-2]. China's 14th Five-Year Plan emphasizes innovation in the integrated circuit sector, highlighting the need for breakthroughs in core technologies. This includes reforms in information and communication, and increased investment in research areas like silicon optical communication and millimeter-wave technology[3-5]. The goal is to translate valuable research of intellectual libraries into affordable chips and systems that effectively serve the public worldwide.

Currently, the " CMOS Radio Frequency Integrated Circuits (RFIC) " course offered by universities nationwide primarily covers fundamental concepts of RF design, design points of basic circuit modules, and practical components based on simulation software. Therein, the practical aspects of utilizing simulation software mainly involve the use of Cadence and other simulation tools to model standalone modules of RF circuits, such as power amplifiers, mixers, and low-noise amplifiers. Beneficially, this approach enables students to master software usage while understanding the design processes of certain RFIC modules and becoming familiar with basic design methods for implementing RF integrated circuits. Due to the constraints of course duration and the assessment complexity, a complete RF transceiver system design is often too time-consuming and challenging for students to fulfill within the allotted course time. Inevitably, a systematic design and simulation of receivers is hardly applied to the curriculum cultivation program of graduate schools throughout the country. Therefore, this course, tailored for the postgraduate students in our university, focuses on modeling and simulating the mixer-first receiver (MF-RX) frontend to enhance students' systematic understanding of the receiver design specifications while mastering the utility of commonly employed software from Cadence IC suites. This aims to forge postgraduate students' professional perspectives in systematic RFIC design. Moreover, the

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extremity goal of research work of universities is to monetize that in industries undoubtedly. Another benefit that should not be neglected recklessly is to feed students some planned cutting-edge knowledge, instead of the basic or even nearly obsolete circuit examples widely available in any textbooks, emphasizing the education of fundamental concepts and principles. We thereby handpicked a technical release of receivers from our lab [6-8], to teach and train the students' capability of systematic design. This tentative is expected to strengthen their innovation ideology and spawn the enthusiasm of challenging unknown realms.

2. Principle of simulation-based experiment

CMOS receiver frontend design focuses on low-noise amplification using LNAs to enhance weak signals while minimizing noise, with careful impedance matching to maximize power transfer[9-12]. It employs mixers for frequency conversion, often down-converting RF signals to intermediate frequencies[13-16]. Integrated filters help eliminate unwanted frequencies, while digital signal processing capabilities enhance signal quality and perform demodulation[17-18]. Power efficiency is crucial, particularly for battery-operated devices, achieved through techniques like dynamic voltage scaling. The design must ensure linearity to handle a wide range of input signals without distortion, and optimize the overall noise figure for better signal-to-noise ratio. High levels of integration in CMOS technology allow for system-on-chip designs, combining multiple functions on a single chip, thereby reducing size and cost while improving performance. A receiver frontend usually includes LNAs, mixers, baseband (BB) amplifiers, and frequency dividers.

Nowadays, the receiver is evolving towards lower noise and power, good linearity, and frequency re-configuration[19-21]. Particularly, the MF-RX frontend has drawn much attention from the industry and academia, due to its performance advantage over conventional LNA-first (LF) receivers. Its primary specifications include frequency range, input matching, conversion gain, noise figure, power consumption, and linearity[22-25]. The frequency range refers to the spectrum coverage that the RX can operate. Good input matching is beneficial for maximizing signal transfer and minimizing reflections. The noise figure describes the additional noise degradation added to the desirable signal transfer. Linearity reflects the receiving ability resilient to undesirable interferences. Power consumption represents the energy consumed during operation.

3. Content of the experiment

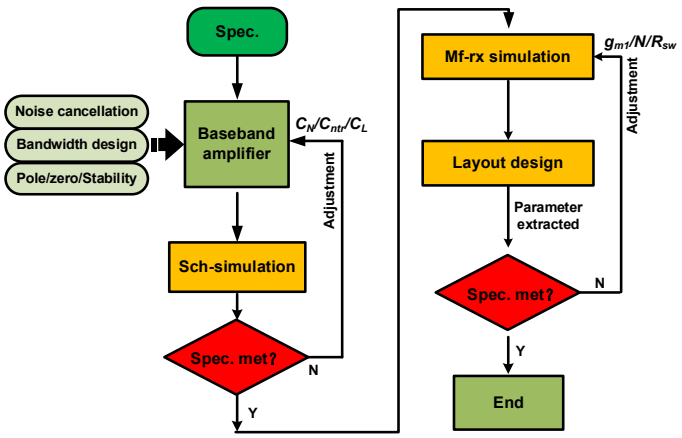

Figure 1: Design workflow.

Experimental Objective: This experiment aims to conduct a research experiment on an MF-RX frontend, utilizing a 65 nm CMOS process and showcasing the overall RX metrics. Students will gain proficiency in operating integrated circuit software, Cadence Virtuoso Suite. They are in expectation to complete the entire design encompassing schematic editing, layout design, and systematic simulation, thereby enhancing the practical skills of troubleshooting in the integrated circuit discipline.

Experimental Requirements: During the practical process, students are to understand the specific meanings of the technical specifications and to master the design methods for the MF-RX frontend. Based on the CMOS 65 nm process, the design must meet the core specifications: fRF =1-3 GHz, BB BW>200

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MHz, Gain = ~30 dB, NF < 2.5 dB, IB-IIP3 > -15 dBm, and Power = ~30 mW.

When designing the circuit, the first step is to decompose the systematic specifications and estimate the requirements for the BB amplifier. Namely, noise cancellation (NC), bandwidth (BW) design, and pole/zero allocation must be well planned prior to getting the simulation of the BB amplifier started. Once the theory work is done, we move to the practical simulation with the Virtuoso tool, doing DC, AC, and STB simulations. If the results do not meet expectations, an adjustment is then conducted on the parameters of CN/Cntr/CL. Once the performance is met, a systematic simulation is further executed. Typically, DC simulation is first performed to check the quiescent point of mixer switches and the BB amplifier. Secondly, the kinds of simulation: PSS/PSP/PAC/QPSS/QPAC are simulated to acquire electrical performance. Finally, based on the optimal schematic parameters, the layout is drawn and arranged. According to the updated post-simulation results, an iterative adjustment is applied to parameters gm1/N/Rsw to ensure that the systematic performance meets the specification requirements. The specific process is illustrated in Figure 1.

3.1 Input impedance and conversion gain

If the parasitic is neglected, as in Figure 2(a), the RX input resistance is approximately written as

$$R_{in} = R_{sw} + \frac{2}{\pi^2} R_{bb} = R_{sw} + \frac{2}{\pi^2} \frac{1}{g_{m1}} \tag{1}$$

The coefficient $2/\pi^2$ is derived from a local oscillator (LO) stimulus with a duty cycle of 25% [22-25]. In this context, R_{sw} and R_{BB} represent the switches' resistance and the input BB resistance, respectively. The parameter g_{m1} refers to the transconductance of the transistor M_1. In Figure 2(a), R_s indicates the source resistance of the antenna. To achieve input matching, the condition R_s=R_{in} typically needs to be satisfied. In this scenario, the CG stage's resistance is regarded as matching impedance, in contrast to the CS stage serves to mitigate the CG stage's noise.

In Figure 2(b), the parameters V_{sb} and R_{sb} represent the equivalent signal and resistance observed towards the mixer orientation. It is important to note that the BB signal travels through the primary path, where it is in-phase amplified through the CG stage and phase-reversed by the CM stage, ultimately coming to the output v_o. Conversely, the BB signal of auxiliary path is conveyed in the opposite phase, then reaches the output. Overall conversion gain combining both paths is illustrated below.

$$Gain = \frac{-1}{1 + g_{m1} R_{sb}} \left(N g_{m1} + g_{m2} \right) r_o \tag{2}$$

N symbolizes the scaling ratio of M_3/M_4, and g_{m2} stands for the transconductance of M_2. The output resistance r_o takes $r_{o2}//r_{o4}//R_L$.

3.2 Noise cancellation comparison

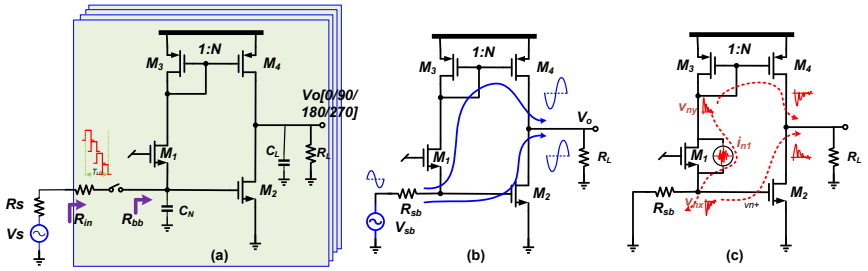

Figure 2: (a) MF-RX macro-model (b) Signal flowing paths. (c) Noise cancellation paths.

Since initially proposed by Twente University, the common-gate (CG) common-source (CS) topology, as a popular structure, has been widely used in various receivers where the low noise delivered by the embedded NC trait is highly desirable [26-30]. The NC principle is illustrated in Figure 2(c), and one just checks the noise behavior of in1, by transistor M1. It flows along two paths: one portion of in1, flows upward into the CM and then appears at the output. Alongside, the noise voltage vnx generated by the same in1, also flows to the output along an auxiliary path via M2. The opposite polarity of the two noise outputs thus cancel each other, perfectly, provided the following relationship is met,

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$$i_{no} = \Delta i_{n1} R_{sb} g_{m2} - \Delta i_{n1} \frac{g_{m4}}{g_{m3}} = \Delta i_{n1} R_{sb} g_{m2} - \Delta i_{n1} N \tag{3}$$

Namely, $N=R_{sb}g_{m2}$ where Rsb is the source resistance. For a certain CM ratio, N, a larger R_{sb} accordingly requires a smaller g_{m2}, or less power in equivalence. So, using the NC at BB is more power efficient than at RF since a smaller resistance of 50 Ω is universally adopted in an RF NC case.

Table 1 RF/BB NC Comparison

NC@RF side	Para.	g_{m1}	g_{m2}	R_s	N
	Value	20 mS	70 mS	50 Ω	3
NC@BB side	Para.	g_{m1}	g_{m2}	R_{sb}	N
	Value	3.5 mS	41 mS	286 Ω	5.8

To see this point, an RF/BB NC comparison is conducted using simulations and summarized in Table 1. A conventional RF NC, requires that the R_s takes 50 Ω, and then transconductance g_{m1} equals 20 mS. By taking typical N=3 and adopting g_{m2}=70 mS leads to the NF=2.1 dB. However, in the BB NC with ~6x larger BB resistance R_{sb}, the g_{m1} is reduced proportionally. So is the g_{m2} due to the factor N. DC Power is thus saved while maintaining the low NF level.

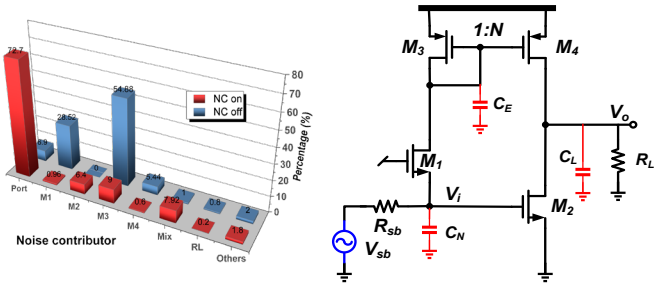

Figure 3: (a) noise cancellation histogram. (b) Simplified model for bandwidth analysis.

To conceive the NC effectiveness in the RX circuit, a simulation comparison is conducted, related to noise. Using the Cadence simulator, the simulation combination of PSS+PNOISE is conducted, where the fundamental tone fixes at a typical 2 GHz. Then at the Virtuoso panel, we print out the noise summary data at the interested inband (IB) frequency point, as plotted in Figure 3(a). The comparison clearly shows that the NC effect nullifies the M_1 contribution, leaving the input port as a predominant contributor. In contrast, the M_1/M_3 along the main path yields an overwhelming noise output even larger than the input port, once the auxiliary path is turned off.

3.3 Bandwidth analysis and simulation

Neglecting the switches' parasitic influence, the BW is thus mainly determined by the BB NC circuit. Figure 3(b) shows the simplified BB circuit model, including lumped capacitance equivalence for the convenience of analysis. Specifically, the C_N, C_E, and C_L are for the N-path capacitor, CM parasitic, and load. Then, one deduces a transfer function (TF) as

$$TF = \frac{v_i}{v_{sb}} \frac{v_o}{v_i} = \frac{1}{R_{sb}\left(\frac{1}{R_{sb}} + g_{m1} + sC_N\right)} \frac{g_{m2}\left[g_{m3}\left(1+\frac{Ng_{m1}}{g_{m2}}\right)+sC_E\right]}{g_{m3}+sC_E} \frac{1}{\frac{1}{r_o}+sC_L} \tag{4}$$

The resulting three real poles and single zero are further displayed below.

$$p_1 = \frac{\frac{1}{R_{sb}} + g_{m1}}{2C_N},\ p_2 = \frac{g_{m3}}{C_E},\ p_3 = \frac{1}{r_o C_L},\ z_1 = \frac{g_{m3}\left(1+\frac{Ng_{m1}}{g_{m2}}\right)}{C_E} = p_2\left(1+\frac{Ng_{m1}}{g_{m2}}\right) \tag{5}$$

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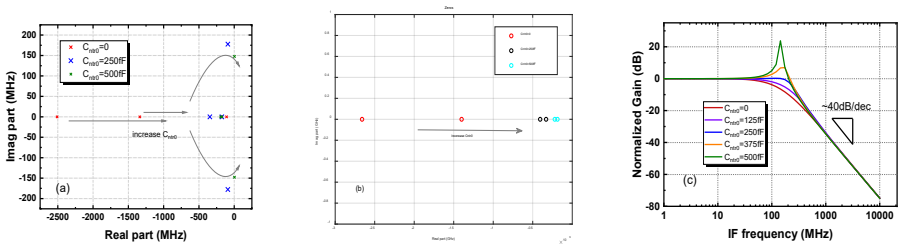

Figure 4: Manipulation on (a) poles, (b) zeros, and (c) BBTF.

The zero generation is due to the coexistence of the CG stage and the CM-slow path, and the CS stage-fast path. Unfortunately, this method gains simplicity but ignores the Miller capacitance effect on poles/zeros. Moreover, the pure real poles also bring no benefit in BW extensions alongside a low Q of ~0.5[31-32]. Thus, we resort to a spectre-simulating tool for accessing accurate pole distribution.

Meanwhile, to double the power efficiency, the circuit in Figure 2 evolves into complementary n/pMOS structures[33-35], provided in Figure 5. Ultimately, the BB circuit based on stacked n/pMOS structures is simulated to check the zeros/poles and TF traits. We configure the P/Z simulation option in the Cadence tool and set up input/output terminals, and run the schematic level simulation. Once finished, we plot the results directly and see that there are four poles and two zeros, as shown in Figure 4(a)&(b). It defies the speculation from the above equations. More beneficially, appending a neutralized capacitor C_{ntr0} converts the two real poles of them to a conjugate pair. Meanwhile, the left poles are roughly canceled by the two real zeros. In short, a second-order filter turns out. We further perform AC simulation of the Cadence tool and set up the interested frequency range and input/output terminals to acquire TF results. Figure 4(c) just illustrates the resulting curve towards the C_{ntr0} variations. Notably, A 40 dB/dec rolling-off appears. Another impressive trait is that tuning C_{ntr0} will regulate the quality factor and the BW range. What is more, The C_{ntr1} addition also has a similar function of BW extension and Q improvement. The optimal simulation indicates that the C_{ntr0} and C_{ntr1} take 250 and 120 fF, preferably.

3.4 Simulation of RX performance

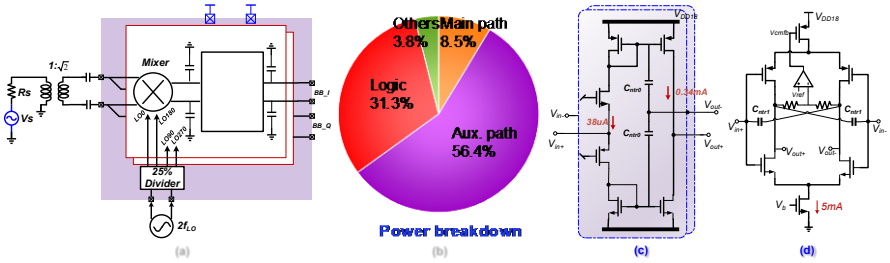

Figure 5: (a) MF-RX schematic and (b) power breakdown. (c) Main path and (d) auxiliary path.

Displayed in Figure 5(a) is the experimental schematic of MF-RX frontend in 65 nm CMOS. The sub-circuits are given in Figure 5(c) and 5(d), such as the main/auxiliary path. Especially, 25% duty-cycle LO clocks are enabled by a frequency divider, fed by a sole 2x sinusoidal input frequency source, and using two cross-connected D-latches and compact Nand gate logic [6,8].

To do an RX performance simulation, we should do a global setup with a period steady-state (PSS) option. Namely, the frequency divider factor takes 2, the fundamental frequency equals that of the sole LO sinusoidal source, harmonic number is chosen >10. A further PSS simulation was conducted to observe the DC spectral distribution at the voltage supply, and then the circuit power consumption was computed. Figure 5(b) just depicts the power breakdown, where the DC power of signal path burns 21.9 mW from a 1.8 V supply while the dynamic power of the divider takes ~10 mW/GHz, with another 1.2 V supply.

Thereafter, to simulate the input matching metric, we need additional PSP setup, where the cared sideband takes zero, and the frequency range takes 1 GHz. A simulation is then performed. Figure 6 shows the simulated input reflection, S11, when the fLO is consecutively adjusted from 1 to 3 GHz. Meanwhile, to plot the gain result, we configure an option of sideband taking -1 in the PAC panel and keeping the PSS panel as set before. Figure 6(b) just displays the resulting 33 dB voltage gain with a

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bandwidth of ~220 MHz under the 2 GHz LO stimulus. Different from the flat gain in Figure 4(c) with tuned neutralized capacitors, the small overshooting here is potentially caused by parasitics of C_{ntr0} and C_{ntr1} incurred in layout design. Generally, the larger BB BW design catering to a high data rate also scales down the CN and CL greatly, saving the area budget. To evaluate the noise metric, we set up a PNOISE panel as appropriate, where output terminals take RX's output ports, and sideband taking -1 denotes a down conversion to BB. The simulated result is captured accordingly. Figure 6(c) illustrates that the simulated NF result at fLO= 2 GHz is below 2.7 dB, adjacent to the upper edge of passband. The minimum NF is recorded as low as 2.2 dB at f_{IF}=50 MHz. In comparison, when the auxiliary path is disabled, the NF shows ~8 dB degradation. This further supports the verification of BB NC.

Due to the positive feedback from neutralized capacitors, careful stability checks are necessary. A current probe was inserted into the feedback loop of the inverter in the auxiliary path, and a PSTB simulation was conducted, with the probe and ground locations predetermined. The resulting data curve, shown in Figure 7(a), indicates that the loop gain remains significantly below 0 dB throughout the IF range, ensuring stability. Additionally, another positive feedback inside the main path was also assessed and found to be stable, although this is not presented as a separate figure.

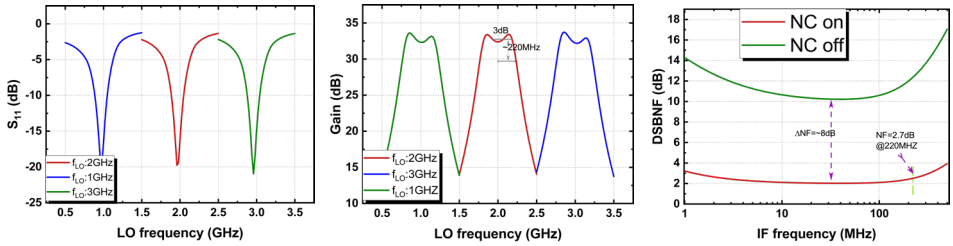

Figure 6: (a) Input reflection, S11. (b) Conversion voltage gain. (c) Noise figure.

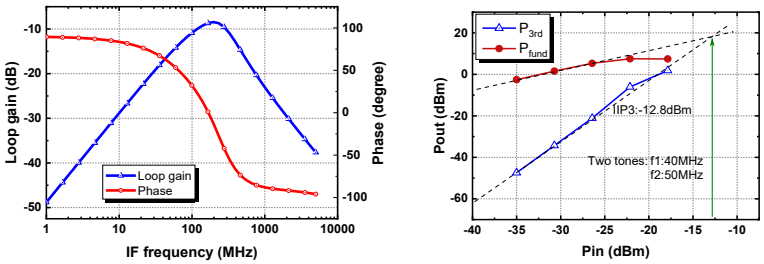

Figure 7: (a) Stability simulation results. (b) In-band linearity plot.

Linearity is also evaluated by Cadence tools. The IP3 metric is commonly used to describe distortions of circuits[36-40]. But a simulation of QPSS+QPAC is needed here for receivers. In QPSS panel, we set f_{LO} and f_{RF} input as large and moderate tones, respectively; the harmonics of them are 10 and 5, respectively. Then in the QPAC panel, we set up an AC input with point frequency adjacent to the frf input at QPSS panel. So, a two IF tone of f_{IF1}/f_{IF2}=40/50 MHz resulted under 2 GHz f_{LO} for example. Turning to the schematic, we open the RF input port and edit its property, where the large signal RF power and the AC power input are both configured as the same variable p_{rf}, then the simulation is performed by sweeping the p_{rf} between -30 and 0 dBm, typically. Once finished, we open the menu: direct plot/QPAC result, and select the proper third-order items for the IF output. The result then prompts instantly and indicates an IB IIP3 of -12.8 dBm roughly, as shown in Figure 7(b). The linearity is deduced to be limited by the non-ideal virtual ground nets, $V_{in+/-}$ (Figure 5(c)), seen by the larger IB interferences, inevitably creating unwanted voltage swings at BB input and contributing distortions. Although the auxiliary stage cancels the main path's distortion following the NC principle, the inverter, however, produces addon distortions by itself.

4. Conclusion

An integration of theory and practice in the "CMOS Radio Frequency Integrated Circuits" course significantly enhances students' learning experiences. By utilizing the Cadence Virtuoso suite for simulation practices, students gain hands-on experience that complements their theoretical knowledge, particularly in the design and simulation of RF receiver frontends. This methodology not only spawns deeper engagement and enthusiasm for the subject but also equips students with essential skills to bridge

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the gap between theoretical concepts and practical applications. As a result, the course effectively prepares postgraduate students for career challenges, ultimately fostering the overall quality of education in the CMOS RF integrated circuits curriculum.

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