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Chip-Package Power Integrity Co-Analysis Based on Chip Power Model

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Abstract: *Chiplet package technology brings the advantage of high integration and miniaturization, meanwhile power supply ripple noise of chiplet has become an important index that must be considered in package design. In order to control the low-voltage and high-current power supply ripple noise of a high-performance processor chip, package designer adopts the chip-package power integrity co-analysis method based on Chip Power Model (CPM) to realize the ripple noise and impedance simulation of the chip-package system power network. Based on the co-design, the optimal decoupling capacitor addition strategy is obtained, and the ripple noise of the system power is optimized.*

Keywords: *Chip Power Model, Chip-Package Co-Simulation, Power Supply Ripple Noise*

1. Introduction

Currently, digital processing chips such as processors and Field Programmable Gate Arrays (FPGAs) are continuously evolving towards low power consumption, which is accompanied by a continuous decrease in the power supply voltage. At the same time, the improvement of chip computing power and the exponential growth of computing units have led to a continuous increase in the power supply current. As a result, on the one hand, the power supply has become increasingly sensitive to noise ripple. On the other hand, it has imposed increasingly stringent impedance requirements on the power delivery network (PDN) composed of the on-chip power supply, packaging substrate, and Printed Circuit Board (PCB)[1][2].

The power supply ripple noise originates from the high-frequency impedance characteristics of the PDN[3]. Whether it is the chiplet design, packaging design, or PCB design, it is required that the frequency-domain impedance curve of the PDN be smooth, and that it meets the characteristic impedance value requirements calculated from the power supply noise tolerance within the required frequency band[4]. Due to the limitation of the finite planar area, the impedance curve of the PDN often has multiple resonance points, resulting in the impedance near the resonance frequency being much higher than the characteristic impedance[5]. And the decoupling capacitor is a design optimization measure specifically taken to counteract the impedance resonance at specific frequency points[1][6]. Usually, chip design, packaging design, and PCB design engineers add decoupling capacitors based on the impedance analysis results of their respective design parts (i.e., the on-chip power grid, the power plane of the packaging substrate, and the power plane of the PCB), to ensure that the impedance curve is smooth in the frequency bands they are concerned about[6][7].

There are two main problems with the above traditional design method: Firstly, this method lacks an intuitive verification of the system power supply ripple noise. Secondly, according to the serial design process of chip design, packaging design, and PCB design, when the PDN impedance is relatively high, the margins of the packaging design and PCB design will be compressed layer by layer, and there may even be a situation where the PCB design is difficult to meet the PDN requirements[8][9][10]. Based on the above problems, from the perspective of packaging design, this paper adopts a joint simulation method based on the CPM model to achieve the collaborative analysis and suppression of the PDN ripple noise of the chip-packaging substrate part. The results show that through joint simulation and collaborative analysis, the PDN ripple noise problem can be solved more accurately compared with the traditional design method.

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2. Chip Power Model

The Chip Power Model (CPM model) is a model proposed by Ansys Corporation for dealing with the time-domain noise analysis of the chip power delivery network (PDN)[11]. Essentially, the CPM model is in the format of a SPICE netlist, which includes the RLC parasitic parameters of the chip bumps and the transient load current model of the bumps described by the Piece-wise linear (PWL) waveform. In short, the CPM model provides a PDN sub-circuit model of the chip bumps and the on-chip transient current load. By combining it with the PDN model of the packaging substrate, the joint PDN simulation of the chip and packaging and the time-domain noise simulation can be achieved[12][13]. An example of the CPM model is as shown in Figure 1.

1.Definition of die bump group

```
* VDD_Bump_1_4_0     :   (5330.000000 300.000000)    :   PAR_0_0_VDD      = PAR_0_0_VDD
* VDD_Bump_1_12_3    :   (6930.000000 300.000000)    :   PAR_0_0_VDD      = PAR_0_0_VDD
* VDD_Bump_2_1_5     :   (4730.000000 400.000000)    :   PAR_0_0_VDD      = PAR_0_0_VDD
* VDD_Bump_3_7_8     :   (5930.000000 600.000000)    :   PAR_0_0_VDD      = PAR_0_0_VDD
* VDD_Bump_3_16_10   :   (7730.000000 700.000000)    :   PAR_0_0_VDD      = PAR_0_0_VDD
* VDD_Bump_4_9_15    :   (6330.000000 800.000000)    :   PAR_0_0_VDD      = PAR_0_0_VDD
```

2.Definition of Chip PWL current source

```
* CPM Port Name | Average current (A) | Max. magnitude of current | Net voltage *
* PAR_0_0_VDD 0.00339626 0.0137393 1.1
* PAR_0_0_VDD_x 1.49017 10.753 1.1
* PAR_0_0_VDD_y 3.61718 17.7291 1.1
* PAR_0_0_VSS -5.11075 28.4681 0
* Average power = 5.62181 W.

Icursig1 PAR_0_0_VDD 0 pwl(
+ 0.000000ps    0.0034036629
+ 50.000000ps    0.0024161326
+ 80.000000ps    0.0037725254
+ 110.000000ps    0.0043664716
+ 140.000000ps    0.0053210847
+ 170.000000ps    0.0048333133
```

3.Sub-circuit model of Chip PDN

```
* No connection to global ground (Spice node 0) *
C0_1 PAR_0_0_VDD PAR_0_0_VSS 2.46333052825e-11
R_1_1 PAR_0_0_VDD n5 57.1162396124
C_1_1 n5 PAR_0_0_VSS 1.27568221796e-12
R_2_1 PAR_0_0_VDD n6 13.0272790247
R_3_1 PAR_0_0_VDD n6 1688000
C_2_1 n6 PAR_0_0_VSS 9.54671815482e-12
C0_2 PAR_0_0_VDD_x PAR_0_0_VDD 1.20597397039e-11
```

Figure 1: Content of CPM model.

3. Process of Chip-package Co-simulation based on CPM model

Simulation tools such as SIwave and Sigrity provide the function of importing the CPM model. Using these tools, the bumps in the model can be mapped one-to-one with the bump pads on the packaging substrate according to their coordinate positions, and circuit ports can be generated on the bump side. At the same time, the simulation tools offer the function of converting the RLC sub-circuit model in the model into the S/Y/Z parameter model of the PDN. This allows the sub-circuit model on the chip side to be directly cascaded with the PDN of the packaging substrate in the simulation tool. By following the conventional simulation method for frequency-domain impedance, the joint PDN impedance curve of the chip-packaging substrate can be obtained[13]. Keep your text and graphic files separate until after the text has been formatted and styled. Do not use hard tabs, and limit use of hard returns to only one return at the end of a paragraph. Do not add any kind of pagination anywhere in the paper. Do not number text heads-the template will do that for you.

Moreover, since the CPM model itself is in the SPICE netlist format, which is equivalent to a current source plus an RLC sub-circuit model, the CPM model can be imported into circuit simulation tools such as ADS and Ansys Circuit Designer and cascaded with the PDN S-parameter model of the packaging

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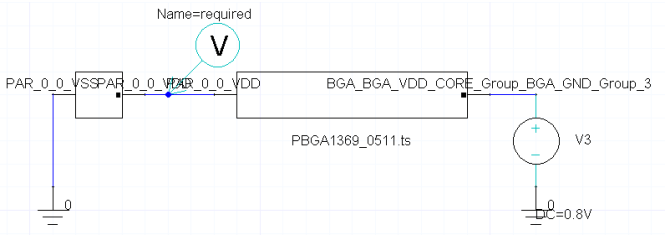
substrate. Through transient simulation, the transient power supply voltage waveform on the joint PDN of the chip-substrate can be obtained, that is, the power supply ripple noise simulation. The simulation circuit diagram is as shown in Figure 2[13].

In this paper, Ansys SIwave electromagnetic field simulation tool is used to conduct the joint frequency-domain impedance simulation of the chip and packaging, and the Ansys Circuit Designer time-domain simulation tool is used to carry out the power supply noise ripple simulation.



Note: In the above block diagram, the voltage source model represents an ideal VRM, which can be replaced by the IBIS model of a voltage regulator chip.

Figure 2: Circuit diagram of power ripple noise simulation.

4. Co-simulation and Co-analysis of signal processing Chiplet package

The research object of this paper is a high-performance signal processing Chiplet and its plastic packaging substrate. The large Chiplet mainly includes four processor chips, two FPGA chips (one main and one auxiliary, and the auxiliary FPGA is specifically used for the synchronization and data exchange among the four processors) and four DDR modules. The core power supply VDD_CORE of the main FPGA and the power supplies VDD_CLU0~3 for the four processors have a power supply voltage of 0.8V, while the power supply AVCC_RXTX for a high-speed IO interface has a power supply voltage of 0.95V; each of these six groups of power supplies corresponds to a GND. Since a large instantaneous current will be generated when the computing units in the signal processing Chiplet operate simultaneously, it is necessary to carefully evaluate the frequency-domain impedance and time-domain ripple noise of the power supply to ensure the normal operation of the chip under extreme conditions. The packaging designers need to ensure that the noise ripple of the five groups of power supplies does not exceed 5% through appropriate power plane division and the addition of decoupling capacitors. In order to realize the joint PDN simulation and analysis of the chip and packaging, the chip backend engineers have extracted the CPM models of the five groups of power supplies.

The processor chip studied in this paper uses a 16-layer ABF plastic packaging substrate. VDD_CORE and VDD_CLU0~3 are respectively located directly below the main FPGA chip and the four processor chips, and the power supply AVCC_RXTX for the high-speed Serdes interface is located on the left side of the substrate, corresponding to the position of the LGA lead-out terminal. A relatively large area of the power plane is divided to reduce the DC voltage drop and noise ripple of these six groups of power supplies. The situation of the plane division is shown in Figure 3. Based on the CPM model, this paper obtains the joint PDN impedance curve of the chip and packaging, and compares it with the result obtained from the simulation of the packaging substrate alone. Subsequently, the noise ripple of each group of power supplies is obtained, and decoupling capacitors are added specifically to reduce the noise.

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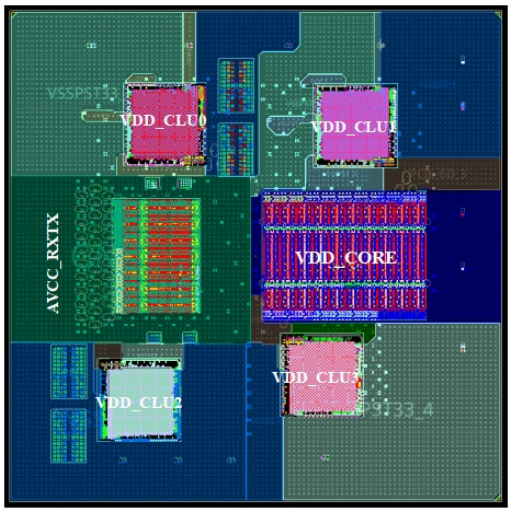
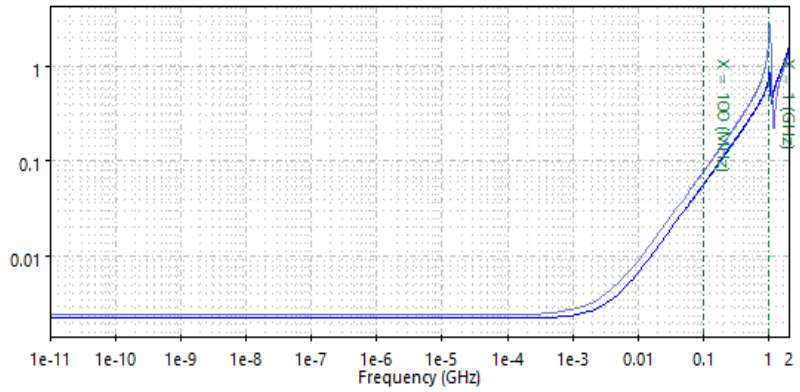


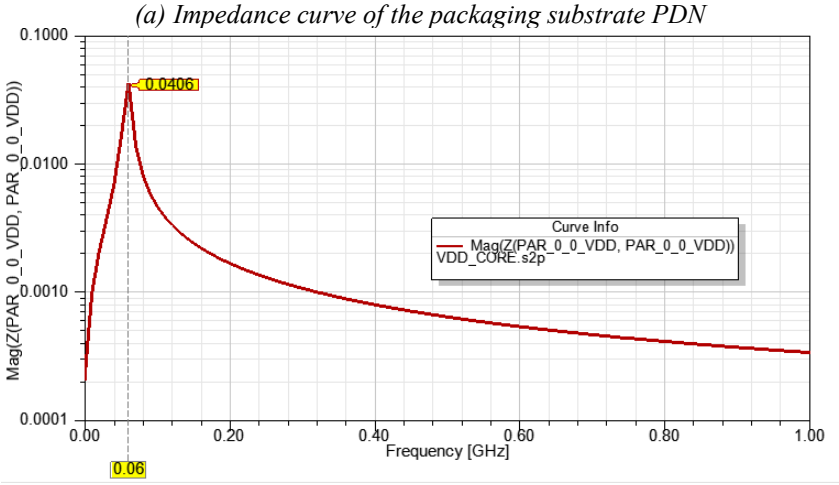
Figure 3: Power Partition Design of the Packaging Substrate for the Processor Circuit.

4.1 Frequency-domain impedance simulation

Based on the process introduced above, the SIwave electromagnetic field simulation software was used to simulate the joint frequency-domain impedance of the chip and packaging for each group of power supplies and the individual frequency-domain impedance of the packaging substrate. Taking VDD_CORE as an example, the results are shown in the Figure 4(a)(b) respectively.



(a) Impedance curve of the packaging substrate PDN



(b) Impedance curve of the packaging substrate PDN

Figure 4: Simulation results of VDD_CORE PDN impedance curve.

From the results, it can be seen that there are significant differences between the PDN impedance curve obtained from the simulation of the packaging substrate alone and the curve obtained from the joint simulation of the chip and packaging substrate. The comparison results show that: 1) After considering

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the influence of the chip PDN, the impedance resonance points shift towards the low-frequency band; 2) After considering the influence of the chip PDN, the impedance curve becomes smoother in the high-frequency band. Based on the PDN impedance analysis and the principle of adding decoupling capacitors:Since on-chip capacitors have smaller parasitic resistance/inductance compared to surface-mounted capacitors, the high-frequency decoupling problem is usually prioritized in the chip PDN design,which is consistent with the results obtained from the joint simulation. High-frequency decoupling capacitors introduce new resonance points in the medium- and low-frequency bands, and the packaging substrate side only needs to solve the decoupling problem in the medium- and low-frequency bands (tens of megahertz to hundreds of megahertz). Therefore, it can be known that conducting PDN impedance simulation by combining the chip and packaging substrate is a more scientific and effective analysis method.

4.2 PDN transient noise simulation

Based on the process introduced previously, the ANSYS Circuit Designer circuit simulation tool was used to simulate the noise ripple of each group of power supplies respectively. Taking VDD_CORE as an example, the results are shown in Figure 5.

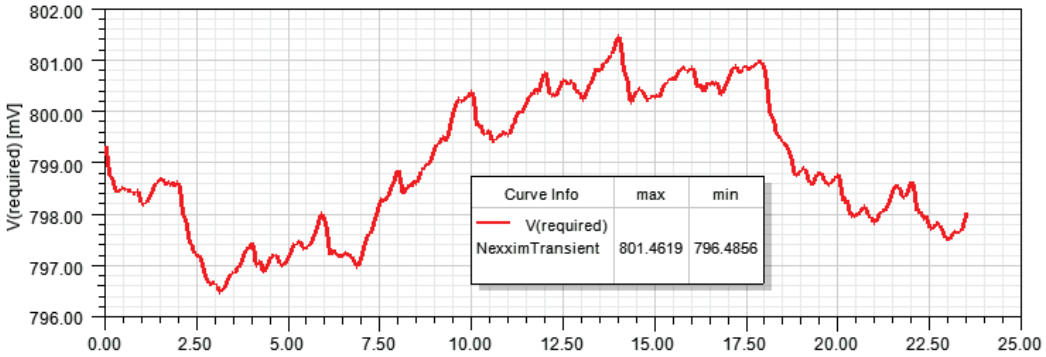

Figure 5: Simulation results of the noise ripple of VDD_CORE.

From the results, it can be seen that there are mainly ripples in two frequency bands on the time-domain waveform of the VDD_CORE power supply voltage. Overall, the voltage fluctuates slightly in an approximate sinusoidal wave of a lower frequency, and a high-frequency ripple is superimposed on this sinusoidal wave. The overall voltage fluctuation is -0.44~0.18%. The discrete Fourier transform is performed on the time-domain voltage waveform to obtain the voltage spectrogram (Figure 6), and the spectrogram verifies our analysis.

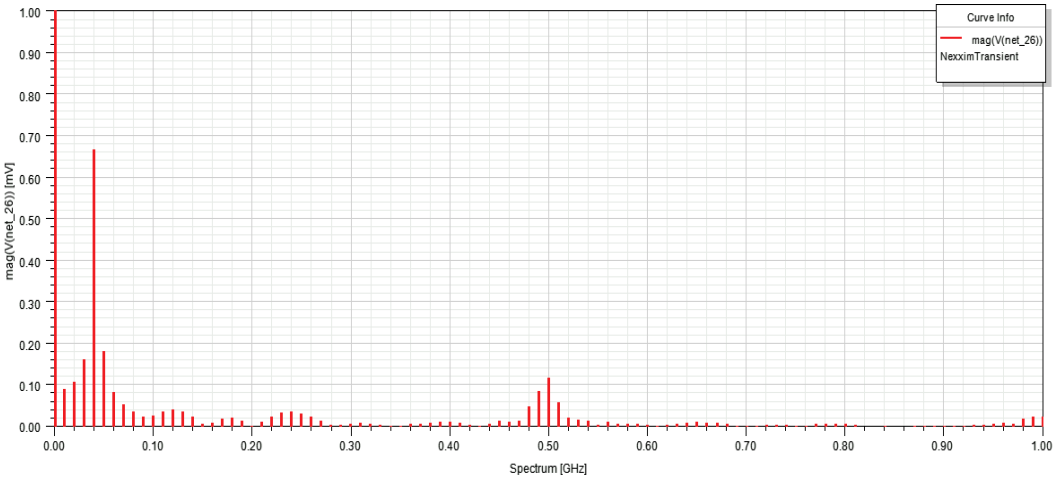

Figure 6: Spectrum of the transient voltage waveform of VDD_CORE.

In the figure, there is significant noise near the frequency points of 40MHz and 500MHz, corresponding to the two types of noise ripples in the time-domain waveform. To further analyze the source of the noise ripples, based on the most fundamental circuit analysis principle: V = IR, that is, the voltage value at each frequency point is equal to the product of the current component at that frequency point and the PDN impedance. The noise ripple can be regarded as the superposition of the noise voltages

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at each frequency point. First, by referring to the VDD_CORE impedance curve (Figure 7) obtained from the previous analysis, it can be found that the noise ripple in the low-frequency band originates from the relatively high frequency-domain impedance in this band.

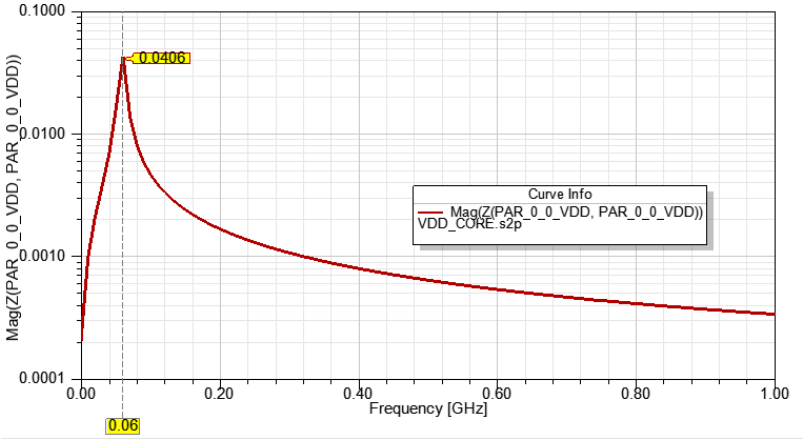


Figure 7: Noise frequency bands corresponding to the VDD_CORE frequency-domain impedance curve.

Further spectrum analysis is carried out on the transient current source model of VDD_CORE in the CPM model, and the obtained transient current spectrum is shown in Figure 8. Obviously, the relatively high transient current component near 500MHz has caused the high-frequency noise ripple of the power supply.

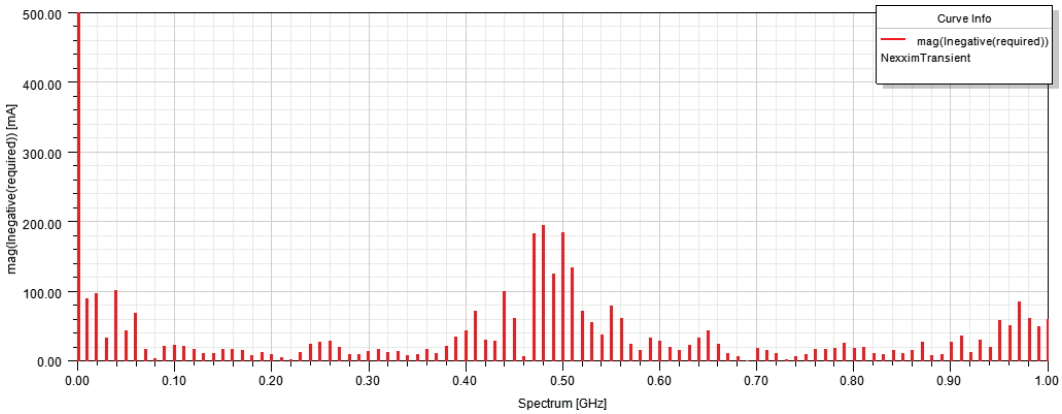
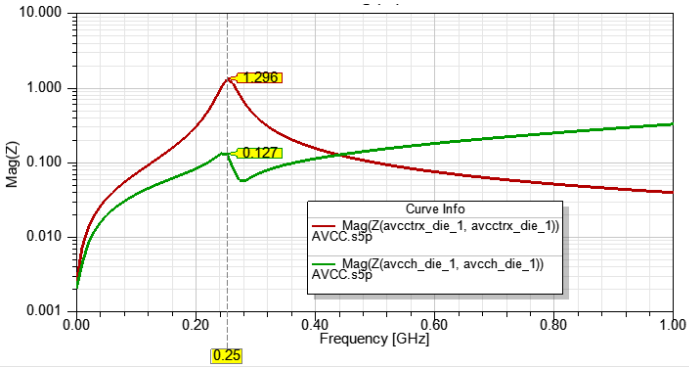


Figure 8: Spectrum diagram of the transient current of the chip power supply.

From this, it can be concluded that the power supply noise ripple is simultaneously related to both the transient current spectrum and the PDN impedance spectrum. Taking the high-speed IO power supply AVCC_RXTX as an example (Figure 9), the peak value of its frequency-domain impedance curve reaches 1.3Ω, which far exceeds the requirements of conventional impedance control. However, due to the relatively small transient current component in the corresponding frequency band, the voltage fluctuation is only-1.2% to 1.6%, which can still meet the design requirements.



(a) Joint frequency-domain impedance curve of the AVCC_RXTX chip-package

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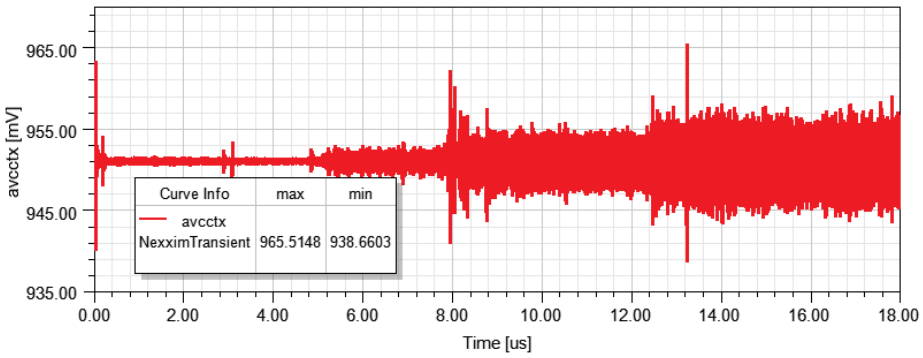
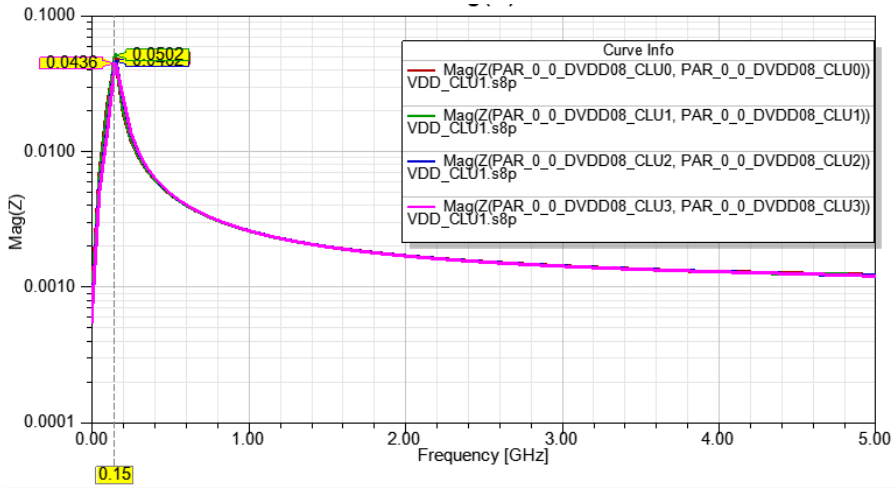


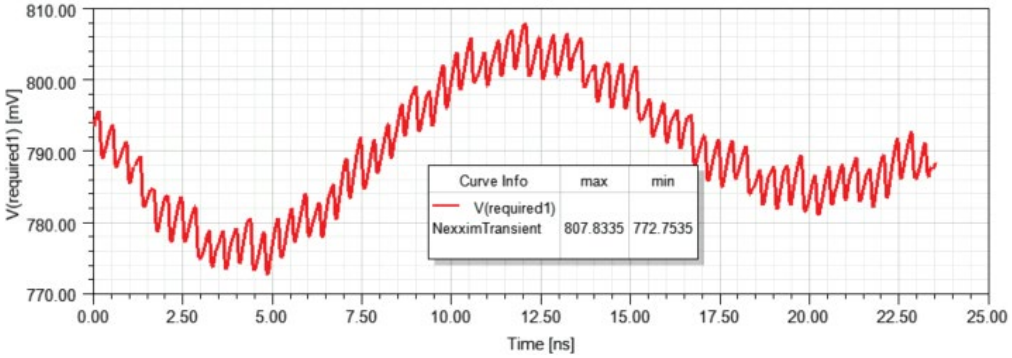
(b) Transient voltage waveform of AVCC_RXTX

Figure 9: Examples where the frequency-domain impedance is relatively large, but the transient voltage waveform meets the requirements.

In contrast, taking the processor power supply voltage VDD_CLU0 as an example (Figure 10), the peak value of its frequency-domain impedance curve is only about 50mΩ. However, due to the large transient current, its voltage fluctuation reaches -3.40% to 0.98%, and optimization is recommended. In conclusion, the time-domain waveform analysis based on the chip-packaging joint simulation can provide more intuitive and accurate analysis results than the traditional impedance analysis method, while avoiding over-design.



(a) Joint frequency-domain impedance curves of the VDD_CLU0~4 chips and their package



(b) Transient voltage waveform of VDD_CLU0

Figure 10: Examples where the frequency-domain impedance is relatively small, but the transient voltage waveform exceeds the requirements.

4.3 Power supply noise optimization

Based on the previous analysis results, this paper proposes three noise optimization measures: 1) Reduce the peak value of the chip transient current; 2) Reduce the peak value of the PDN impedance; 3) Ensure that the frequency band of the chip transient current peak does not coincide with the resonance

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point of the PDN impedance. These three measures are jointly completed by chip design and packaging design engineers. Chip design engineers are responsible for controlling the frequency points of the transient current peak and adding on-chip high-frequency capacitors, while packaging design engineers are in charge of controlling the resonance points of the PDN impedance and adding decoupling capacitors on the substrate.

This paper also takes the VDD_CLU0 power supply as an example for power supply noise optimization. Based on the frequency-domain impedance curve obtained from the joint simulation, the impedance resonance frequency is analyzed to be 150MHz. Still using the conventional method of adding decoupling capacitors, capacitors with a self-resonant frequency near 150MHz are selected, and through multiple iterations, the final decoupling capacitor scheme is obtained as follows: 2 capacitors of 10nF and 1 capacitor of 4.7nF (Figure 11). After adding the decoupling capacitors, the fluctuation of the power supply transient power drops to -2.91% to 0.59% (Figure 12), which is an improvement of about 20%.

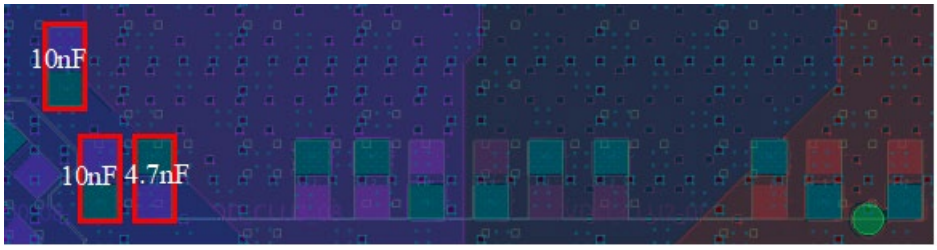

Figure 11: Decoupling capacitors of VDD_CLU0.

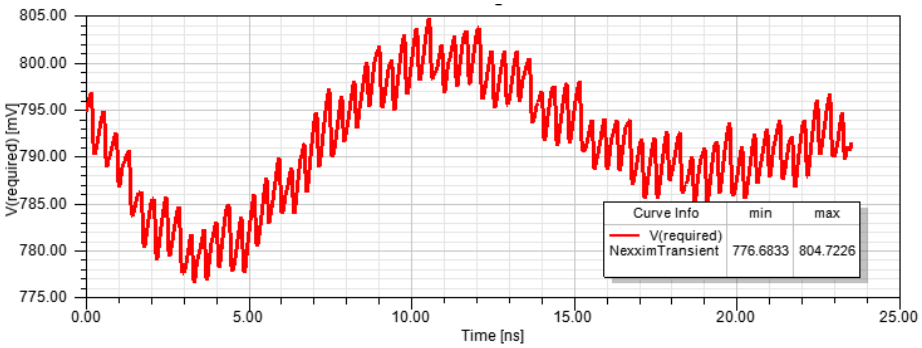

Figure 12: . Optimized results of the noise ripple of VDD_CLU0.

The above optimization method was adopted to add decoupling capacitors to the packaging substrates of each power supply of the processor, and the transient waveforms were simulated. The results are shown in Table 1. After optimization, the voltage fluctuation of each power supply does not exceed 5%, all of which meet the conventional design requirements.

Table 1: Decoupling capacitor addition of the packaging substrate for the processor power supply and the transient fluctuation range

Power	Capacitors	Noise ripple
VDD_CORE	None	-0.44%~0.18%
VDD_CLU0	10nF×2, 4.7nF	-2.91%~0.59%
VDD_CLU1	10nF×2, 4.7nF	-2.64%~0.60%
VDD_CLU2	10nF×2, 4.7nF	-2.45%~0.86%
VDD_CLU3	10nF×2, 4.7nF	-2.35%~0.87%
AVCC_RXTX	10nF, 100nF	-1.2%~1.6%

5. Conclusions

Based on the previous chip-packaging PDN joint simulation and result analysis, the following conclusions can be drawn:

Based on the chip's CPM model and the S-parameter model of the packaging substrate, a chip-packaging joint PDN simulation can be realized, and the joint frequency-domain impedance and transient voltage fluctuations can be obtained.

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Usually, high-frequency decoupling capacitors are added on the chip side, which causes the resonance point of the PDN frequency-domain impedance to shift to a lower frequency. Only through the chip-packaging joint simulation can the real PDN frequency-domain impedance curve be obtained. The decoupling frequency bands that the packaging substrate focuses on are the medium and low frequency bands (usually 20MHz to 200MHz). In the case of lacking chip design information, the common capacitance values of decoupling capacitors are 0.1μF (30 MHz), 10nF (90 MHz), and 1nF (300 MHz).

When the design space of the packaging power supply is small, the power supply noise can be effectively controlled by avoiding the coincidence of the frequency-domain impedance resonance frequency and the transient current frequency.

The analysis of the frequency-domain impedance and the noise ripple are mutually verified. The noise ripple is the fundamental indicator, and the frequency-domain impedance is used for auxiliary judgment.

In the future, with the increasing complexity and requirements of integrated circuit design, the decoupling design of the power network needs to be jointly completed by chip and packaging design. Chip designers are responsible for controlling the transient current value and adding high-frequency decoupling capacitors, while packaging designers are responsible for medium and low-frequency decoupling and simulation verification.

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