ISSN 2522-6398 Vol. 8, Issue 5: 177-183, DOI: 10.25236/FER.2025.080526

Enhancing Student Engagement in RF Integrated Circuit Course through Simulation Practices Using Cadence and EMX

Benqing Guo[1,a,*], Yuanyuan Shi[1,b], Yao Wang[2,c], Huifen Wang[3,d], Haishi Wang[1,e], Tianbao Wang[1,f]

[1]*Microelectronics School, Chengdu University of Information Technology, Chengdu, China*
[2]*School of Electrical and Information Engineering, Zhengzhou University, Zhengzhou, China*
[3]*School of Civil Engineering and Architecture, Henan University of Technology, Zhengzhou, China,*
[a]*rficgbq@gmail.com,* [b]*yyshi@cuit.edu.cn,* [c]*ieyaowang@zzu.edu.cn,* [d]*wanghuifen2008@sina.com,*
[e]*whs@cuit.edu.cn,* [f]*wangtianbao@cuit.edu.cn*
**Corresponding author*

Abstract: *This paper presents the integration of theory and practice in the course "Radio Frequency Integrated Circuits," emphasizing the importance of both theoretical knowledge and practical software applications. The simulation practices of RF circuits are highlighted as a means to deepen students' understanding of theoretical concepts. The exploration of teaching methodologies utilizing Cadence and EMX simulation software aims to enhance student engagement and enthusiasm for learning. By focusing on the voltage-controlled oscillator module, the study models the entire circuit design and simulation process, enabling students to acquire a comprehensive understanding of RF system simulation design. This approach not only lays a solid foundation for future studies but also seeks to improve students' capabilities in integrating theory with practice. Ultimately, the research aims to promote a significant enhancement in the quality of education in "RF Integrated Circuits".*

Keywords: *RF Integrated Circuits, Practical Teaching, Voltage-Controlled Oscillator, Simulation*

1. Introduction

Integrated circuits, as an emerging modern discipline, are characterized by strong specialization, rapid development, extensive coverage, and significant interdisciplinary integration. The advancement of integrated circuits has driven the development of intelligence, digitalization, and industrialization in China [1-2]. Radio frequency (RF) and microwave integrated circuits, as essential parts of integrated circuits, play a vital role in fields such as wireless communication, radar, and the Internet of Things (IoT), serving as a backbone for the development of the information industry in China. The 14th Five-Year Plan proposed by China government is accelerating the steady growth of innovative technology especially featuring the integrated circuit industry. The challenges yet to overcome emphasize the importance of core technology research and breakthroughs in key issues. It calls for the continuous deepening of reforms in the information and communication sector and increased investment in research and development in critical areas, such as silicon optical communication, millimeter-wave technology, and 3d integration. The fabulous vison is to propel the conversion of research outcomes into affordable chips, devices, and systems, ensuring that technology truly serves the people [3-4].

Currently, the "Radio Frequency (RF) Integrated Circuits" course offered by universities nationwide primarily covers fundamental concepts of RF design, key design points of basic circuit modules, and practical components based on simulation software. Therein, the practical aspects of utilizing simulation software mainly involve the use of Cadence and other simulation tools to model specific modules of RF circuits, such as power amplifiers, mixers, and low-noise amplifiers, as well as to verify parameters through simulation. This approach enables students to master software usage while understanding the design processes of specific RF circuit modules and becoming familiar with common techniques and design methods for implementing RF integrated circuits. Due to the constraints of course duration and the assessment of design complexity, a complete RF transceiver system design is often too time-consuming and challenging for students to achieve the full systematic functionality within the allotted course time. Therefore, this course focuses on modeling and simulating the voltage-controlled oscillator

ISSN 2522-6398 Vol. 8, Issue 5: 177-183, DOI: 10.25236/FER.2025.080526

(VCO) module to enhance students' understanding of the design specifications and circuit structures of VCOs while mastering the use of commonly employed software. This aims to cultivate students' capabilities in RF integrated circuit design. The ultimate value of research work of universities is to get monetized at industries with no doubt. Another point that cannot be neglected is to cultivate students with cutting edge knowledge instead of the basic or even nearly obsolete circuits examples available in most of the current textbooks. We thereby handpicked a VCO circuit from the recent reports of our lab [5-7], to teach and train the students' capability of design and troubleshooting. This bold tentative is expected to strengthen their innovation ideology and cultivate enthusiasm of learning and investigating unknown realms.

2. Principle of simulated-based experiment

The primary purpose of a radio frequency (RF) transceiver is to transmit and receive information. As illustrated in Figure 1. The transmitter converts baseband information into a modulated signal, which is then transmitted through a power amplifier and antenna eventually. The receiver just completes a reversed process of transmitter, receiving signals from antenna and demodulating them into baseband signals. Typical transceiver modules include oscillators, duplexers, mixers, filters, power amplifiers, and antennas [8-12]. Thereof, the VCO as a critical module driving the transceiver system, significantly determines the overall performance of the system. With the increasing demands of communication technology, VCOs are evolving towards lower phase noise, higher frequencies, and wider tuning ranges.

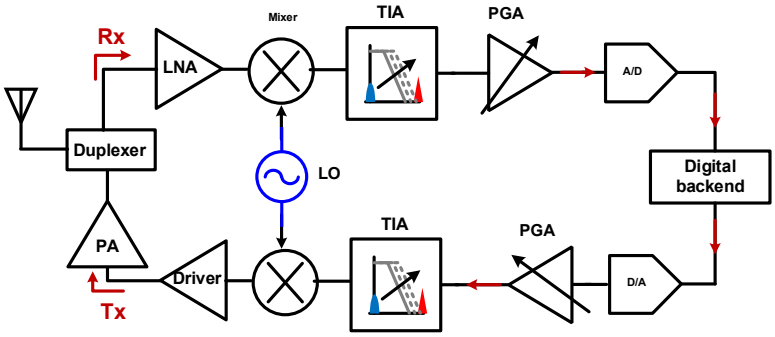


Figure 1: A general transceiver diagram

The design fundamentals of an RF VCO should encompass active devices, and passive devices, to meet the constraints of the design specifications. The insert loss, bandwidth, and impedance transformation of passive devices have a decisive impact on the performance of RF and millimeter-wave integrated circuits. Active devices are also crucial; the biasing state of the transistor determines the operating condition of the VCO. Additionally, the inherent parasitic capacitance of the transistor must be considered and reflected in the circuit parameter design.

The VCO is an oscillator capable of adjusting its output frequency in response to a tuning voltage, widely used in communication and signal processing applications. Its primary specifications include frequency range, tuning sensitivity, phase noise, output waveform, power consumption, and linearity [8]. The frequency range refers to the spectrum of frequencies that the oscillator can generate while tuning sensitivity indicates how responsive the output frequency is to changes in the tuning voltage. Phase noise (PN) describes the frequency stability of the output signal, with lower phase noise indicating better performance. The type of output waveform influences the performance of subsequent circuits, and power consumption represents the electrical energy consumed by the oscillator during operation. Linearity reflects the relationship between variations in tuning voltage and changes in output frequency.

3. Content of the experiment

Experimental Objective: This experiment aims to conduct research on VCOs for key modules in millimeter-wave chips, utilizing a 65 nm CMOS process to design a transformer-coupled 14 GHz VCO. Students will gain proficiency in operating millimeter-wave integrated circuit design software, including EMX and Cadence, and will complete the entire design process encompassing schematic design, layout design, and co-simulation of circuit and electromagnetic fields, thereby enhancing the practical skills of students in the integrated circuit discipline.

ISSN 2522-6398 Vol. 8, Issue 5: 177-183, DOI: 10.25236/FER.2025.080526

Experimental Requirements: During the practical process, students are expected to understand the specific meanings of the technical specifications of VCOs and to master the design methods for VCOs. The design must meet the following core specifications: operation in Class F mode, a center frequency of ~14 GHz, an output swing greater than 1 V, a tuning range exceeding 12 %, and the PN less than -115 dBc/Hz at a 1 MHz offset.

In designing the VCO, the first step is to determine the design specifications for the VCO, followed by the design of the resonant tank and the parameter optimization of the three-coil transformer. Subsequently, DC simulation is performed to establish the transconductance and dimensions of the transistor under reasonable bias voltages. After constructing the schematic and designing the switched capacitor array, the S-parameters of the transformer are co-simulated. Finally, based on the schematic parameters, the layout is drawn and arranged, with iterative adjustments made according to the simulation results to ensure that the performance of the designed circuit meets the design requirements. The specific process is illustrated in Figure 2.

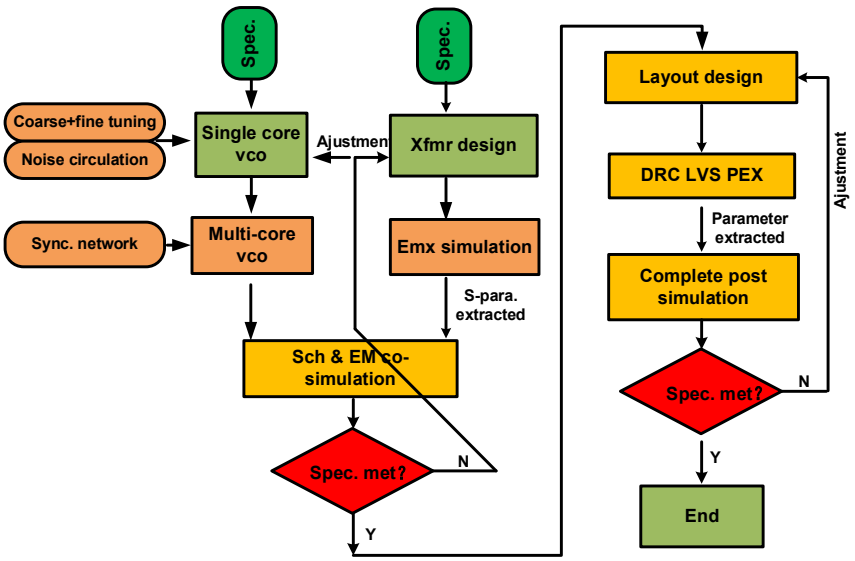


Figure 2: Design workflow of a VCO

3.1 Transformer design and simulation

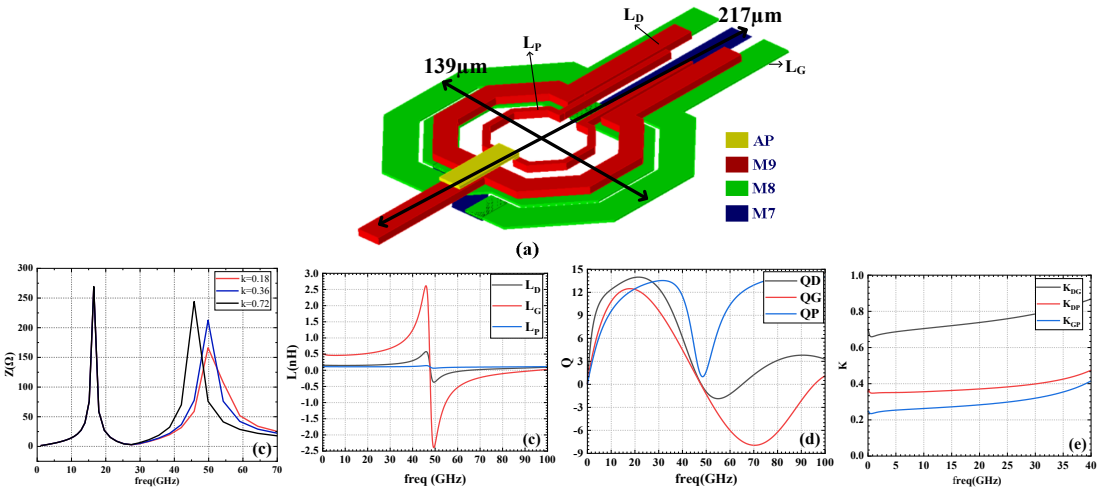


Figure 3: (a) Transformer structure. (b) Resonant impedance curves of different kDP values

Three coil parameter results of (c) inductance value L, (d) quality factor Q, and (e) coupling coefficient k.

Transformers are widely utilized in circuit modules such as VCOs, mixers, and frequency doublers [13-16]. Integrated on-chip transformers leverage mutual inductance between multiple conductors to

ISSN 2522-6398 Vol. 8, Issue 5: 177-183, DOI: 10.25236/FER.2025.080526

transfer alternating current from one coil to another, achieving impedance matching to reduce power loss. When designing by EMX software, it is desirable to route the transformer trace in topper thick metal layers, often employing an octagonal structure with vertical coupling to enhance the quality factor (Q) .

Upon completing the layout, electromagnetic (EM) simulation is necessary to obtain the inductance values while considering parasitic effects. The specific simulation results are illustrated in Figure 3, which shows the overall self-inductance values, coupling coefficients, and Q-factor distribution of the coils. Particularly, regarding the oscillator structure in Figure 4, achieving Class F mode operation requires the use of an asymmetric transformer turns ratio of 1 : 1.7 [17]. Furthermore, to effectively drive the tail transistor, the coupling coefficient k of the LD and LP must be appropriately set up. Excessive coupling can lead to shifts in the third harmonic impedance, adversely affecting the normal Class F operation.

3.2 VCO design and simulation

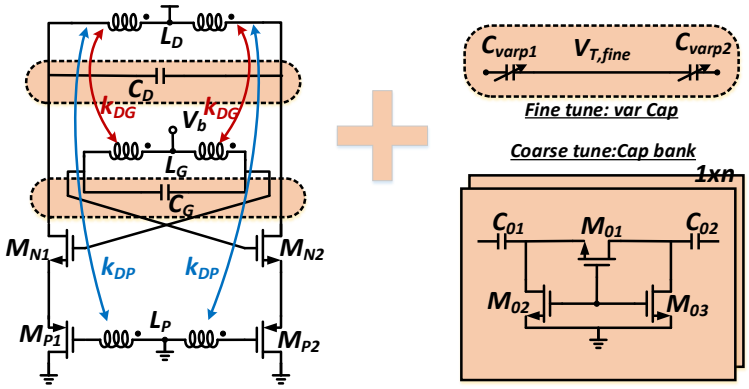


Figure 4: Single core Noise circulating VCO based on tripler transformer coupling

The VCO employs a noise-cancellation structure to achieve noise reduction, utilizing a three-coil transformer coupling to operate in Class F mode, which further reduces phase noise. Coarse tuning of the frequency is implemented using digital 4-bit control, combined with fine-tuning via varactor diodes, resulting in a wide tuning range. The specific topology is illustrated in Figure 4. To achieve better PN performance, a multi-core structure is also an effective technical approach. The multi-core extension can be realized through either a resistive direct connection or a mode suppression structure. Compared to the complexity of mode suppression, the resistive direct connection is simpler and more intuitive, making it more user-friendly for students as beginners in the course. A standard supply voltage of 1.2 V is selected, with the sole bias voltage V_b set at 1 V. If V_b is too low, the circuit struggles to oscillate; if it is too high, the circuit enters a voltage-limited region, leading to significantly increased power consumption. Accordingly, a DC simulation is performed to determine the transconductance of the oscillator at equilibrium state. Combining this with the impedance values shown in Figure 3(b), and ensuring the condition $g_m z_{tank}>2$ for oscillation startup, we select the dimensions of the transistors as specified in Figure 5(a).

The principle of noise circulation is referred to in Figure 5(b), where a single-sided circuit is adopted for simplicity of analysis. At the equilibrium state, the noise current injected into the tank is shown as

$$\overline{I_{ALL}^{\ 2}} = n^2 \overline{I_{\mathrm{n1}}^{\ 2}} + m^2 \overline{I_{\mathrm{p1}}^{\ 2}}, \tag{1}$$

Where

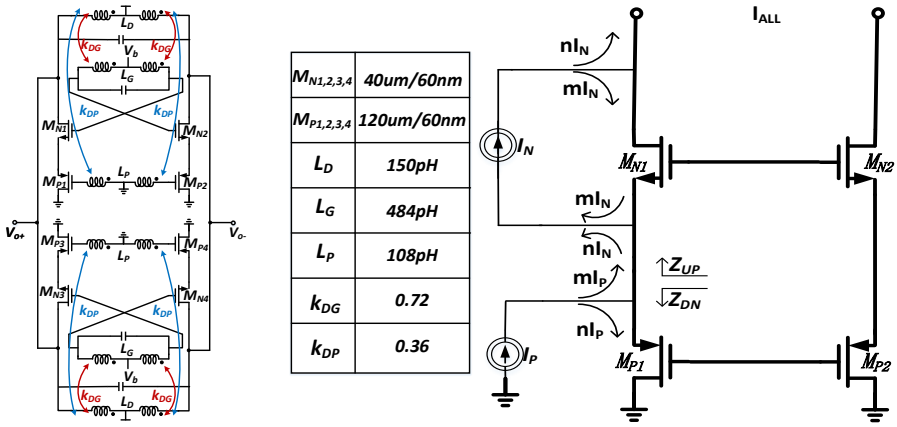
$$m = \frac{Z_{dn}}{Z_{up} + Z_{dn}}, n = \frac{Z_{up}}{Z_{up} + Z_{dn}}. \tag{2}$$

Once the $M_{P1/2}$ in Figure 5(b) is replaced by a single nmos transistor, a conventional oscillator is obtained. At the moment,the corresponding thermal noise again at the equilibrium state is modeled as,

$$\overline{I_{XN}^{\ 2}} = \overline{I_{\mathrm{n,1}}^{\ 2}} \tag{3}$$

ISSN 2522-6398 Vol. 8, Issue 5: 177-183, DOI: 10.25236/FER.2025.080526

When g_{mn}=g_{mp} is taken for an optimal constraint of m=n=0.5. Interestingly, the PSD of the total noise current injected into the tank in Figure 5(b) is only half of the conventional cross-coupled oscillator, thus suppressing the noise of transistors, effectively [18].



$M_{N1,2,3,4}$	40um/60nm
$M_{P1,2,3,4}$	120um/60nm
L_D	150pH
L_G	484pH
L_P	108pH
k_{DG}	0.72
k_{DP}	0.36

(a) (b)

Figure 5: (a) Dual-core VCO diagram and parameters. (b) Diagram for internal noise circulating

Using the circuit design environment in Cadence software, a schematic for the VCO circuit was constructed. The final dual-core structure is depicted in Figure 5, with parameters of the transformer also displayed. External pins were created for the interface, followed by the establishment of a symbol and the construction of a test bench for top-level design simulation. Specifically, the S-parameters obtained from the EMX electromagnetic simulation of the transformer were embedded into an N-port device for co-simulation with the transistor circuit. The resistive loss by metal lines connecting the dual cores was maintained <10 Ω to avoid affecting synchronization between the cores.

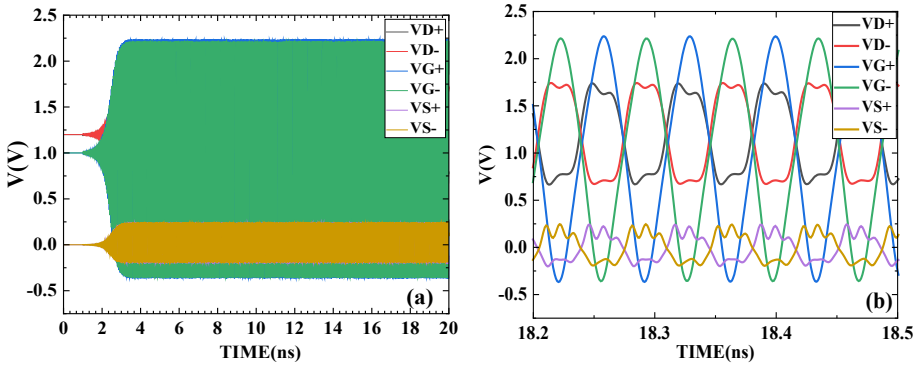


Figure 6: (a) Overall oscillation waveforms and (b) zoom-in waveforms of source, gate, and drain terminals

Using the Spectre simulator of Cadence, appropriate initial node voltage levels for the oscillator were set, followed by transient (trans) simulation with a simulation time length of 20 ns. Upon completion of the simulation, the output waveforms at interested nodes of the oscillator were observed, as shown in Figure 6. A localized zoom-in of the waveforms reveals a square wave approximation at the drain, confirming the Class F operation, with the output node exhibiting a single-ended swing of approximately 1 V, meeting the design specifications. In comparison to the impedance results of the resonant tank in Figure 3(b), a circuit simulation incorporates the parasitic capacitance of transistors. Therefore, when designing the tuning capacitor array, it is essential to account for the parasitics' effect, which is estimated to be in the range of 30 to 50 fF.

Using the Spectre simulator again, a further period steady-state (PSS) simulation was conducted, with the tuning voltage Vt of the varactor diode set as a variable for scanning simulation. By controlling the switches of the 4-bit array, the voltage-controlled effect on frequency variations was achieved, as illustrated in Figure 7(a). The oscillator exhibits approximately a 15 % frequency tuning range, varying from 14.1 GHz to 16.4 GHz. The tuning linearity can be further assessed by calculating the derivative df/dVt from this curve.

The PSS simulation also allows for the evaluation of the impulse sensitivity function (ISF), a crucial

ISSN 2522-6398 Vol. 8, Issue 5: 177-183, DOI: 10.25236/FER.2025.080526

concept to recognize the time-varying noise of the cyclostationary circuits [19-21]. By locating the 'PPV folder' within the 'result browser' directory, the corresponding ISF result curve can be retrieved. As shown in Figure 7 (b), no significant changes are observed at wp=120 μm and 160 μm. Further PN simulation settings were configured in the PNoise panel, with relative frequency offsets ranging from 100 kHz to 100 MHz. The simulation results, displayed in Figure 7 (c), indicate that, as predicted by the ISF, there is no significant PN difference between wp=120 and 160 μm. Consequently, we selected the PMOS dimension as wp=120 μm. Finally, at a 1 MHz offset, the obtained PN is -123.6 dBc/Hz, an impressively low value. At a 1 MHz offset, the corresponding Figure of Merit (FoM) [22-25] is computed as 191 dBc/Hz, using the formula defined below.

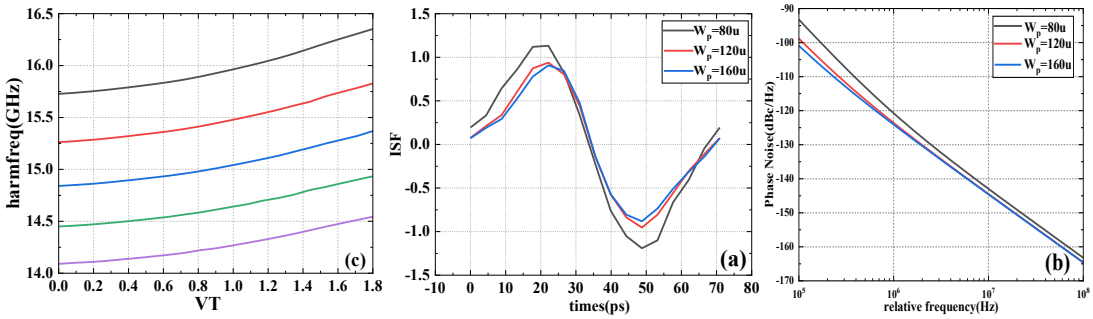


Figure 7: Tuning frequency coverage. (a) ISF curves and (b) phase noise of different tail pMOS sizes

$$FoM = |PN| + 20\lg_{10}\left(\frac{f_0}{\Delta f}\right) - 10\lg_{10}\left(\frac{P_{DC}}{1mW}\right) \quad (4)$$

VCOs, as large signal circuits, also have shown themselves large dynamic currents, or a time-varying quiescent point, quite different from those small-signal circuits with a fixed quiescent point[26-30]. Consequently, one can not get DC power information purely by DC simulation as done in those small-signal circuits. Using the Spectre simulator, a further PSS simulation was conducted to observe the current spectral distribution at the voltage supply node. Specifically, the DC current drained off was recorded, which, when multiplied by the supply voltage, yielded a final power consumption of 36.9 mW.

4. Conclusion

"Radio Frequency Integrated Circuits" is a course that combines theory and practice, requiring students to master both relevant theoretical knowledge and practical software applications. The simulation practice of RF circuits facilitates a deeper understanding and enhancement of the associated theoretical concepts. By exploring the teaching of "RF Integrated Circuits" using Cadence and EMX simulation software, student engagement and enthusiasm for learning can be significantly stimulated. Focusing on the specific module of the VCO, the entire circuit design and simulation process is modeled, allowing students to develop a holistic understanding of RF system simulation design, thereby ultimately promoting a comprehensive improvement in the education quality.

References

[1] Fan, J., & Pang, Z. Talent cultivation program for integrated circuits and integrated systems under the background of "New Engineering" . Modern Education, 2020, 52: 24–28.
[2] B. Guo, H. Wang, Y. Wang, K. Li, L. Li, and W. Zhou, "A mixer-first receiver frontend with resistive-feedback baseband achieving 200 MHz IF bandwidth in 65 nm CMOS," in 2022 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), IEEE, 2022, pp. 31–34
[3] Wang, K., Wei, G., Hong, R., et al. Exploration and reflection on teaching reform of "RF Integrated Circuit" course. Journal of Electrical and Electronic Teaching, 2022, 44(6): 9–12.
[4] B. Guo, J. Chen, L. Li, H. Jin and G. Yang, "A Wideband Noise-Canceling CMOS LNA With Enhanced Linearity by Using Complementary nMOS and pMOS Configurations," in IEEE Journal of Solid-State Circuits, vol. 52, no. 5, pp. 1331-1344, May 2017,
[5] X. Liao, B. Guo, and H. Wang, "A 14.5 GHz Dual-Core Noise-Circulating CMOS VCO with Tripler Transformer Coupling, Achieving-123.6 dBc/Hz Phase Noise at 1MHz Offset," in 2024 IEEE 67th International Midwest Symposium on Circuits and Systems (MWSCAS), IEEE, 2024, pp. 377–381.

ISSN 2522-6398 Vol. 8, Issue 5: 177-183, DOI: 10.25236/FER.2025.080526

[6] C. Li, Y. Wang, B. Guo, T. Chen, and L. Sun, "A 300 nW 10 kHz Relaxation Oscillator with 105 ppm/C Temperature Coefficient," Circuits Syst. Signal Process., vol. 40, no. 11, pp. 5264–5279, Nov. 2021.

[7] J. Chen, B. Guo, F. Zhao, Y. Wang and G. Wen, "A low-voltage high-swing colpitts VCO with Inherent tapped capacitors based dynamic body bias technique," 2017 IEEE International Symposium on Circuits and Systems (ISCAS), Baltimore, MD, USA, 2017.

[8] B. Razavi, RF Microelectronics, Second edition, Prentice Hall, 2012.

[9] Apostolina and D. Manstretta, "A 14.5-17.9 GHz Harmonically-Coupled Quad-Core P-N Class-B DCO with -117.3 dBc/Hz Phase Noise at 1 MHz Offset in 28-nm CMOS," 2022 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Denver, CO, USA, 2022, pp. 211-214.

[10] H. Liu, B. Guo, Y. Han, and J. Wu, "An integrated LNA-phase shifter in 65 nm CMOS for Ka-band phased-array receivers," Int. J. Circuit Theory Appl., vol. 52, no. 5, pp. 2126–2145, 2024.

[11] B. Guo, H. Wang, and G. Yang, "A Wideband Merged CMOS Active Mixer Exploiting Noise Cancellation and Linearity Enhancement," IEEE Trans. Microw. Theory Tech., vol. 62, no. 9, pp. 2084–2091, Sep. 2014.

[12] B. Guo, J. Chen, X. Wang, and H. Chen, "An inductorless active mixer using stacked n MOS/ p MOS configuration and LO shaping technique," Mod. Phys. Lett. B, vol. 32, no. 11, p. 1850129, Apr. 2018

[13] B. Guo and J. Chen, "A mm-Wave Two-Stage CMOS LNA Using Noise Cancelling and Post-Distortion Techniques," in 2024 19th European Microwave Integrated Circuits Conference (EuMIC), IEEE, 2024, pp. 407–410.

[14] B. Guo, H. Chen, X. Wang, J. Chen, X. Xie, and Y. Li, "A 60 GHz balun low-noise amplifier in 28-nm CMOS for millimeter-wave communication," Mod. Phys. Lett. B, vol. 33, no. 32, p. 1950396, 2019.

[15] B. Guo and J. Gong, "A Dual-Band Low-Noise CMOS Switched-Transconductance Mixer with Current-Source Switch Driven by Sinusoidal LO Signals," in 2021 IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), Aug. 2021, pp. 741–744.

[16] B. Guo, X. Wang, and H. Chen, "A 28 GHz front-end for phased array receivers in 180 nm CMOS process," Mod. Phys. Lett. B, vol. 34, no. supp01, p. 2150017, 2020.

[17] M. Babaie and R. B. Staszewski, "A Class-F CMOS Oscillator," in IEEE Journal of Solid-State Circuits, vol. 48, no. 12, pp. 3120-3133, Dec. 2013.

[18] F. Wang and H. Wang, "A Noise Circulating Oscillator," IEEE J. Solid-State Circuits, vol. 54, no. 3, pp. 696–708, Mar. 2019, doi: 10.1109/JSSC.2018.2886321

[19] A Hajimiri, TH Lee, A general theory of phase noise in electrical oscillators, IEEE journal of solid-state circuits 33 (2), 179-194 1998

[20] Benqing Guo, and Guangjun Wen, "Periodic Time-Varying Noise in Current-Commutating CMOS Mixers," Progress In Electromagnetics Research, Vol. 117, 283-298, 2011.

[21] B. Guo et al., "Low-frequency noise in CMOS switched-gm mixers: A quasi-analytical model," IEEE Access, vol. 8, pp. 191219–191230, 2020.

[22] R. Fan, B. Guo, H. Wang, H. Wang, and J. Chen, "A broadband single-ended active-feedforward-noise-canceling LNA with IP2 enhancement in stacked n/pMOS configurations," Microelectron. J., vol. 149, p. 106257, 2024.

[23] B. Guo, J. Gong and Y. Wang, "A Wideband Differential Linear Low-Noise Transconductance Amplifier With Active-Combiner Feedback in Complementary MGTR Configurations," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 68, no. 1, pp. 224-237, Jan. 2021,

[24] B. Guo, G. Yang, and S. An, "A Wideband Noise-canceling CMOS LNA Using Cross-coupled Feedback and Bulk Effect," Frequenz, vol. 68, no. 5–6, Jan. 2014.

[25] B. Guo, J. Ma, and L. Liu, "Detailed investigation of active CMOS mixers noise in submicron technology," Microelectron. J., vol. 42, no. 1, pp. 196–203, 2011.

[26] J. Wu, B. Guo, H. Wang, H. Liu, L. Li, and W. Zhou, "A 2.4 GHz 87 μW low-noise amplifier in 65 nm CMOS for IoT applications," Mod. Phys. Lett. B, vol. 35, no. 32, p. 2150485, Nov. 2021

[27] B. Guo and S. An, "An Analytical Model of Conversion Gain for Submicron Active Mixers with LO Offsets," Frequenz, vol. 67, no. 3–4, Jan. 2013.

[28] B. Guo, H. Wang, H. Wang, L. Li, W. Zhou, and K. Jalali, "A 1–5 GHz 22 mW receiver frontend with active-feedback baseband and voltage-commutating mixers in 65 nm CMOS," IET Circuits Devices Syst., vol. 16, no. 7, pp. 543–552, Oct. 2022.

[29] B. Guo, G. Yang, and X. Bin, "A Differential CMOS Common-Gate LNA Linearized by Cross-Coupled Post Distortion Technique," Frequenz, vol. 68, no. 5–6, Jan. 2014.

[30] N. N. Miral, D. Manstretta, and R. Castello, "A 17-mW 0.5–1.5-GHz Bandwidth TIA Based on an Inductor-Stabilized OTA With 35–42-dBm In-Band IIP3," IEEE Solid-State Circuits Lett., vol. 5, pp. 13–16, 2022.