Design of Resistor Array Drive Controller

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Abstract: A driving controller design which can drive 512×512 resistor array at 200Hz frame rate is proposed. In view of the strict requirements of MOS resistor array drive controller for real-time performance, FPGA, optical fiber transmission card and PC104 technologies are adopted in the design, which studies and solves the two key problems of how to transmit image data at high speed and how to quickly generate multi-channel analog drive signals, and leaves expansion space for the drive control of larger resistor array in the future.

Keywords: IRSP, Resistor array, Infrared

1. Introduction

Infrared imaging hardware in the loop simulation system is a device that can generate infrared images in the laboratory environment and simulate the infrared radiation of the real environment. Its core device is the infrared scene projection device. In terms of infrared scene projection devices, there are mainly resistance array devices, digital micromirror devices (DMD), laser diode array devices, etc. among them, resistance array devices have become the most used infrared scene projection devices due to their excellent performance such as high frame rate, high maximum temperature difference and high gray level. How to drive resistor array to produce high frame rate infrared image is the core problem of constructing infrared imaging hardware in the loop simulation system based on resistor array. Therefore, we need to solve two key problems, one is how to transmit image data at high speed, and the other is how to quickly generate multi-channel analog driving signals [2].

Taking the above two key problems as the core, this paper proposes a design of resistor array drive controller based on FPGA, optical fiber data transmission card and PC104. The drive controller can receive and process the image data sent by the graphics workstation at high speed, generate the resistor array drive control signal and drive 512×512 MOS resistor array.

2. Operating Principle of MOS Resistor Array

The figure is the schematic diagram of a resistor array unit driving circuit. The resistor array adopts a snapshot unit driving circuit, and its working process is divided into three steps. In the first step, S1 is set to low level, m3 is turned on, M2 is turned off, the control voltage Vs sweeps through each column of pixels in the resistor array under the control of the shift register, and the control voltage is stored on the sampling capacitor C1. In the second step, the reset signal CL is set to high level to clear the control voltage loaded by the previous frame image. In the final step, CL is set to low level, S1 is set to high level, and the sampling capacitor C1 starts to charge C2 and heat the resistor R at the same time.

Compared with the traditional scanning resistor array, the snapshot resistor array has a more complex structure, but it can drive all pixels of the resistor array at the same time, and can greatly improve the maximum frame rate. The theoretical maximum frame rate of an 8×128 scale scanning resistor array is 274hz, while under the same other conditions, the theoretical maximum frame rate of the same scale snapshot resistor array can reach 500Hz [3].

Figure 1: Snapshot resistor array unit driving circuit

3. Demand Analysis and Overall Design of Drive Controller

3.1. Real time Requirement Analysis

For 512×512 resistor array requires that the image gray level is not less than 8 bits, so the control voltage level is required to be greater than 8 bits. Considering the influence of noise and voltage drop, 16 bit DA chip can be used for control to meet the requirement of not less than 8 bits. If the resistor array operates at the highest frame rate of 200Hz, the maximum image data throughput is:

$$\frac{512\times512\times16\times200}{10^6\times8} = 104.9\text{MByte/s} \tag{1}$$

It can be seen from the calculation results that the real-time requirements of the drive controller will be extremely strict if the resistance array is to work at the frame rate of 200Hz.

3.2. Overall Design Scheme of Drive Controller

The drive controller adopts PC104 architecture, and the overall design is shown in the figure. Under the control of the upper computer, the driving data is written into the optical fiber transmission card through the PCI Express bus, the control chip of the driving control card reads the data, divides the frequency and synchronously generates the timing control signal from the clock signal output by the crystal oscillator, and then outputs the data and timing control signal to the resistor array respectively.

Figure 2: Overall design of drive controller

4. Realization of High Speed Data Transmission and Design of Drive Control Card

4.1. Clock Synchronization Scheme

The real-time performance of the system and the real-time transmission of image data are actually the problem of completing the specified tasks within the specified time. Whether the real-time performance is realized or not should be measured by time. Infrared imaging hardware in the loop simulation system is a distributed system with two nodes, the time synchronization between nodes is a problem that must be considered. The clock synchronization problem faced by the infrared imaging hardware in the loop simulation system mainly refers to the clock synchronization between the upper computer and the drive control system. How to determine the start of simulation, how to determine the start time of image generation, how to determine the data transmission time, and how to read the data in time are all problems to be faced.

The frame rate of the image projected by the resistor array can be up to 200Hz, and the frame rate of the image generated by the software system can also be up to 200Hz. In the actual simulation process, each subsystem is under the control of different operating systems, and the frame rate of thermal image generated by resistor array scanning must be kept uniform, so the data processing process of each subsystem must be located in mutually independent frame time, and there is a frame delay between them. This delay is allowed in hardware in the loop simulation.

In this scheme, the time synchronization is mainly realized by the method of "single machine timing + query", so that the drive control system becomes the time referee of the whole system, so as to realize the synchronization of simulation. The specific scheme is as follows:

Sending end: the drive controller sends the clock pulse to the fixed area of the optical fiber transmission card in a fixed cycle, and sends a status word along with the clock pulse, which is used to indicate whether there is a new clock pulse. Therefore, the status word is queried before transmission. If other units are not ready to receive clock pulses, the status word is 1, indicating that clock pulses cannot be transmitted. When the status word becomes 0, a clock pulse is sent and the status word is reset to 1.

Receiving end: query whether the status word is 1. If it is 1, it indicates that a new clock pulse has arrived. After reading, set the status word to 0. After the generation of one frame of image is completed, the next query is carried out.

The whole system is precisely timed by the drive controller. According to the frame rate setting of the system, the drive controller sends the frame time clock pulse through the optical fiber. The infrared image dynamic real-time generation and control software running the graphics workstation starts the frame image rendering and generates the infrared image after receiving the clock pulse. The software extracts the image and converts it into the radiation intensity with gray level, and then goes through data conversion and D/A correction, Write the corrected data into the optical fiber transmission card, write the flag bit of image generation completion to the specified address of the optical fiber transmission card, and notify the drive controller that the image generation has been completed. So far, the work of one frame of the graphics workstation is completed, and then the infrared image dynamic real-time generation and control software starts to wait until the arrival of the next clock pulse. After receiving the image generation completion flag, the drive control system drives the resistor array in a subsequent frame, so as to complete the image data output of the simulation computer to the resistor array. The work of the drive controller is to process the corresponding work in another frame time, which does not overlap with the frame time of the image generated by the image real-time generation software system. In this way, the image generation and image display are based on the clock of the driving control system, avoiding the frame loss caused by the accumulation of clock errors between systems.

The above shows that the frame rendering cycle of the infrared image dynamic real-time generation and control software is controlled by the lower computer drive controller, and the image generation time also includes the transmission time of instructions and image data in the optical fiber network, as well as the response time and reading flag bit of the image generation software system.

4.2. Optical Fiber Transmission Card

The optical fiber transmission card is responsible for transmitting the infrared image data generated in real time by the graphics workstation to the lower computer drive controller. After the infrared image

dynamic real-time generation and control software on the graphics workstation generates 512×512 infrared image, configure the register of the optical fiber transmission card to start the hardware DMA, the optical fiber transmission card DMA moves the image data to the memory cache on the board, and the image framing module on the board according to the number of image frames cached in DDR3, frame the image data and send it to the lower computer drive controller drive control card through optical fiber. The optical fiber transmission card is designed with data sending channel and instruction input channel. It can receive the clock pulse sent by the lower computer drive control card through the instruction input channel, and generate the infrared image in real time after receiving the pulse.
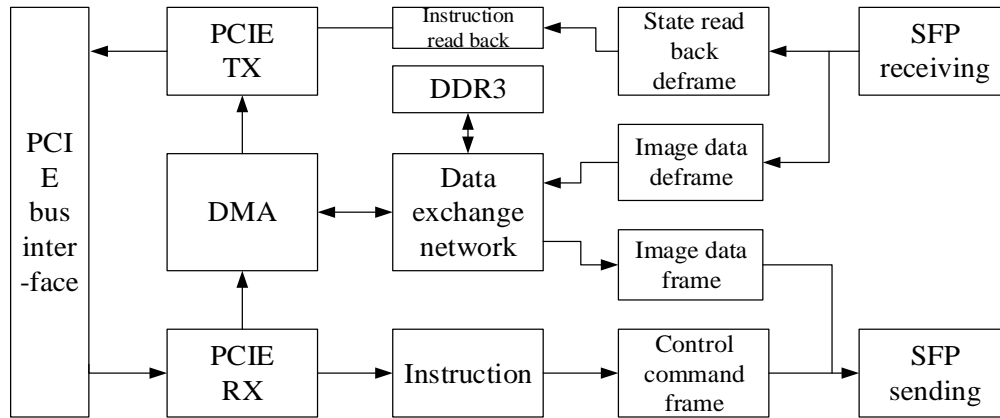

Figure 3: Design schematic diagram of optical fiber transmission card

4.3. Drive Control Card

The main task of the driver control card is to receive the infrared image and generate the driver 512×512 resistor array timing control digital signal and 32 parallel analog control signals. After receiving the data from the fiber data transmission card of the upper computer, the SFP receiving port of the drive control card carries out data processing. The data processing is mainly to deframe the image and carry out non-uniformity correction processing. After the correction processing is completed, the control voltage data is obtained. The voltage data is cached to DDR3 of the drive control card through the DDR3 read-write control module to complete the reception of image data. The drive control card divides the frequency of the external synchronization trigger signal or the clock signal generated by the crystal oscillator to generate a timing signal. In the timing control module, the external synchronization signal can be delayed according to the different internal and external synchronization signals, and the delay time adjustment resolution is 10us. Generate timing signal required by the resistor array, and combined with the DAC control logic, read out the current frame voltage data from DDR3, control the DAC conversion and generate 32 analog drive signals of the resistor array. Its working principle is shown in the figure.
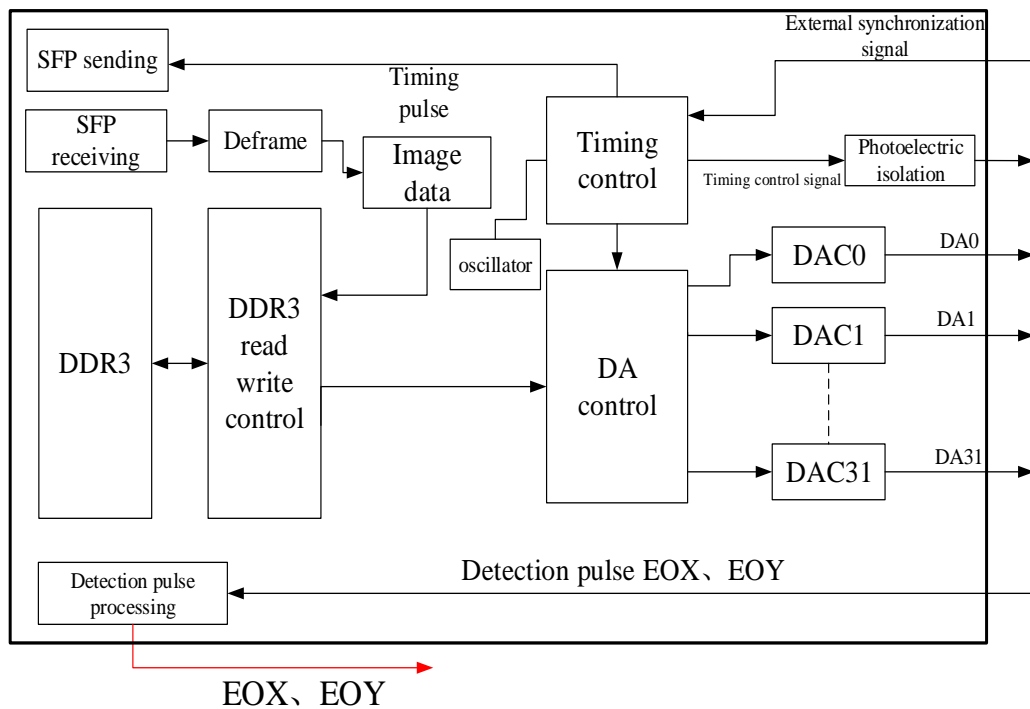
Figure 4: Principle diagram of drive control card

4.4. High Speed Generation Technology of Multi-Channel Analog Driving Signal

At the beginning of simulation, the upper computer starts to produce infrared images after receiving the clock pulse of the drive control card, then transmits the image data to the cache of the optical fiber transmission card through hardware DMA, and writes the flag bit at the specified address of the optical fiber transmission card. At this time, the time spent is no more than 5ms. At the beginning of the second frame, the optical fiber transmission card deframes the data of the first frame and sends it to the drive control card through the optical fiber. After receiving the image data of the first frame, the drive control card de frames, performs non-uniformity correction processing, generates control voltage data, and caches the data in the DDR3 module of the drive control card. Under the control of the timing control module, the DA control module reads out the control voltage data in DDR3 and generates 32 parallel analog drive signals. Under the control of the timing control signal, the 1st row, 17th row, 33rd row... 481st row of the first column of the resistor array are gated to charge the sampling capacitors of the selected 32 pixels. At this time, the time spent $T1 = 0.57us$. After charging the sampling capacitors of the first batch of pixels, gate the second row, the 18th row, the 34th row... The 482nd row of the first column and charge the sampling capacitors of the selected 32 pixels again, and so on. After $T2=17\times T1=9.69$ us, the sampling capacitors of the first column of the resistance array will be charged, and the last T1 time will be used as redundancy. After $T3=513\times T2=4.971$ ms, the sampling capacitors of all pixels of the resistance array will be charged, The last T2 time is used as redundancy. After the sampling capacitors of all pixels are charged, the timing control signal will clear the control voltage of the previous frame on all pixels and light all pixels synchronously to complete the driving control of one frame.

When driving and controlling the first frame, the upper computer has generated the infrared image data of the second frame and transmitted it to the cache of the optical fiber data transmission card through DMA. After the drive control of the first frame is completed, the drive control card will complete the drive control of the second frame, and the upper computer will complete the image rendering and writing of the third frame. By analogy, it can be seen that the data generation, writing and driving control are completed at the same time in one frame, but there is always a delay of one frame in both works.

5. Conclusions

Focusing on how to transmit image data at high speed and how to quickly generate multi-channel analog driving signals, the design of resistor array driving controller based on FPGA, optical fiber transmission card and PC104 technology is studied. After testing, the drive controller can complete the high-speed reception and processing of image data, quickly generate multi-channel analog drive signals, drive 512×512 MOS resistor array to the maximum frame rate of 200Hz, and leave expansion space for driving and controlling larger resistance array in the future.

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