International Journal of Frontiers in Engineering Technology
ISSN 2706-655X Vol.4, Issue 7: 26-29, DOI: 10.25236/IJFET.2022.040706

Design of multi-channel data acquisition system based on FPGA

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Abstract: *FPGA has been widely used in data acquisition and processing in modern industrial production and scientific research due to its integration of VLSI and programmable devices. In this paper, a multi-channel data acquisition system based on FPGA is designed to meet the requirements of data acquisition in aircraft power supply inspection. The designed system realizes the conversion from FPGA local bus to PCI bus through PCI9054 bridge chip, and then completes the connection and communication between the data acquisition system and the upper motherboard through PCI bus. The system debugging results show that the designed system can realize the data acquisition and processing function.*

Keywords: *FPGA, data acquisition, PCI bus*

1. Introduction

With the deepening of industrial technology and science and technology research, the requirements for data acquisition also increase, data acquisition system not only need to have efficient data transmission rate, but also need high-performance processors to make accurate and fast data processing. Field Programmable Gate Array (FPGA) is highly integrated, easy to use and fast to improve performance. Therefore, FPGA can be used to complete low-cost and low-power data acquisition system design in a short time.

Aiming at the application of aircraft power supply system ground inspection, this paper designs a multi-channel data acquisition system based on FPGA. The data analysis and data display part of the system are completed by the upper computer software, and the data acquisition process is realized by THE FPGA logic.

2. Hardware design

2.1. System hardware composition

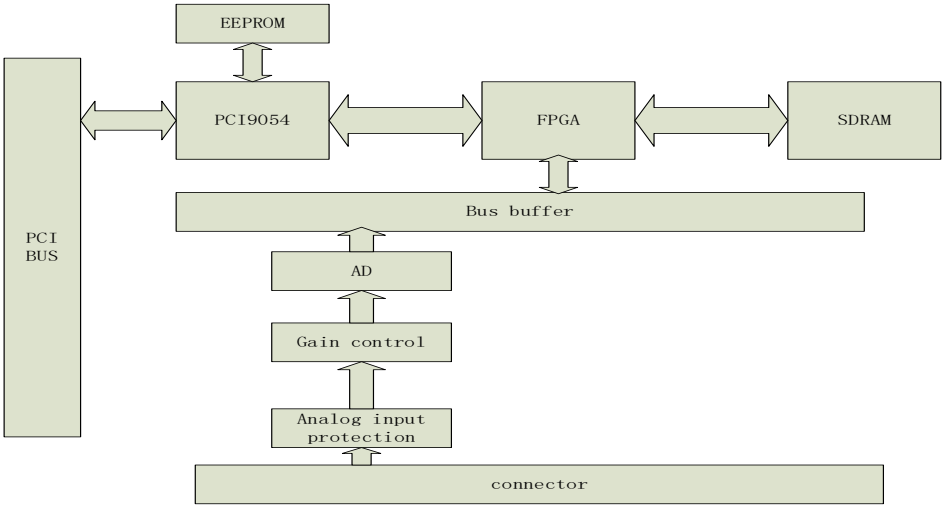

Figure 1: Overall system design block diagram

ISSN 2706-655X Vol.4, Issue 7: 26-29, DOI: 10.25236/IJFET.2022.040706

The system should take into account the bad environment factors, especially the external temperature fluctuations, so the FPGA chip's working characteristics should be good enough to maintain the wide temperature working characteristics; At the same time, in order to meet the requirements of multi-channel data transceiver, signal level conversion chip and other devices to complete circuit connection, the NUMBER of I/O pins is required to be at least 300. Therefore, spartan-6 series, a cost-effective FPGA chip developed by XILINX Company, is selected. The overall design block diagram of the system is shown in Figure 1.

2.2. Design of each module of the system

2.2.1. Main control unit module

In FPGA configuration circuit design, M0 and M1 are used to set FPGA configuration mode. In the circuit, M0 is connected to high level and M1 is connected to low level, which can make FPGA work in main series mode. For the needs of program debugging, JTAG mode is also set, TDI and TDO are the data input and output pins of JTAG respectively.

2.2.2. Data acquisition Module

In the design of signal acquisition circuit, the USE of AD7606 chip design, AD7606 and FPGA between the use of 16-bit parallel connection. The AD7606 can simultaneously sample all analog input channels. When two CONVST pins are connected together, all channels are sampled synchronously. Two CONVST inputs can be controlled using a single CONVST signal. Each analog input pin is surrounded by AVCC analog power pins and AGND pins. In this design, THE AD chip works with an external reference voltage source, and the reference voltage input pin needs to be decoupled by a decoupling capacitor.

In the analog input protection circuit, the resistor plays the role of voltage distribution; Small signal diode and TVS tube play the role of over-voltage protection. When the analog signal of the current 12 channels input is greater than 60V or less than -60V, and the last 20 channels input is greater than 30V or less than -30V, TVS tube will clamp the voltage at ±12V to prevent the analog switch from burning out. Figure 2 shows the specific design.

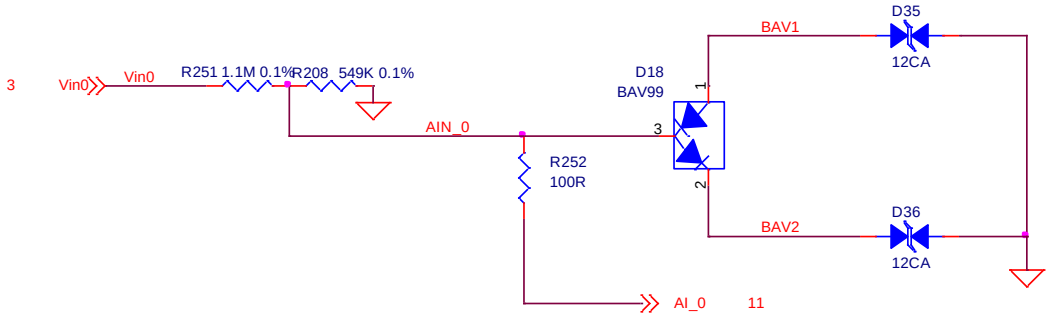

Figure 2: Analog input protection circuit

In the analog switching circuit, the analog input is required to be 12 channels single-ended, 20 channels single-ended /10 channels differential optional. In the circuit design, 32 channels of analog input are selected by two 161 switching circuits respectively, and the switch chip controls the signal switching of even channels and odd channels and the single-ended/differential switching of two functions.

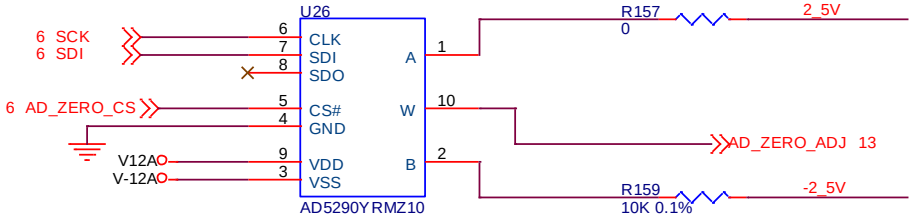

Figure 3: Zero bias calibration circuit

In order to ensure that AD meets the specified accuracy requirements, the card uses a digital potentiometer to calibrate its accuracy. The digital potentiometer communicates with FPGA through SPI,

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and writes different values to the digital potentiometer to make it show different resistance values or partial voltage characteristics, so as to achieve the effect of calibration circuit.AD calibration includes zero bias calibration and gain calibration. See Figure 3, Figure 4.

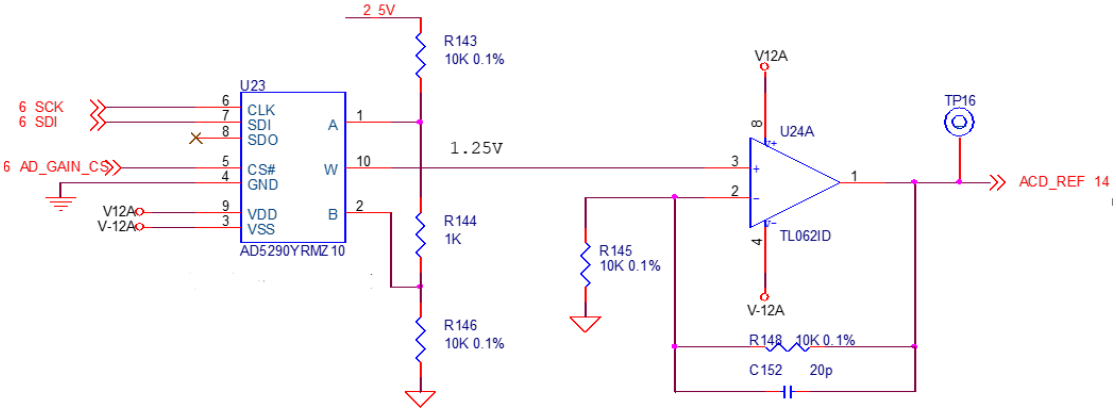

Figure 4: Gain calibration circuit

3. The software design

The main content of this chapter is the logic design of FPGA firmware. In the top-level module of FPGA logic program, it is mainly divided into three parts, including data storage module, sampling process module and control module.

The sampling module is used to realize the timing sequence logic of data acquisition. In the control of AD acquisition process, when the multifunctional analog signal board is powered on, A pulse signal is output to the CONVST A of AD chip through FPGA. The ADC conversion of both V1 and V2 starts at the rising edge of CONVST A, at which time the signal BUSY output is high, indicating that AD is converting. When the signal BUSY output is low, it means that the conversion from analog signal to digital signal has been completed, and the converted data is stored in the external SRAM. When the data is read, CS chip selection signal is set low, and the converted data is output to the data bus in sequence with the low level pulse of RD. When the data collected by two parallel channels is put on the data bus in turn, it represents the completion of a signal acquisition, conversion and reading.

The data storage module transmits the collected data to the memory chip, and a large amount of data needs to be cached by SDRAM memory. Therefore, an SDRAM controller needs to be designed inside FPGA to realize the control of off-chip SDRAM and complete the storage of multi-channel data. The main function of the control module is the relation between the time sequence of data transmission and the FIFO between receiving and sending.

The control module needs to define the communication protocol between upper computers and determine the relationship between address and data. When the bus receives data, the upper computer initializes it first, and then determines the channels and parameters for receiving data. The data is transmitted to FPGA through PCI bus according to the defined protocol. After triggering the channel, the collected data is sent to the upper computer according to the standard instructions.

4. System testing

During debugging, the data acquisition function of the designed data acquisition and processing system is verified by signal generator. During the test, the logic is written into the FPGA configuration chip, and 5V power supply is provided to the designed acquisition system. The interface of the signal generator is connected with the clock signal and data signal of the acquisition card in turn, and the input and output signals are observed with oscilloscope.

5. Conclusion and Analysis

FPGA has been widely used in the industrial field because of its advantages of fast data transmission and strong expansibility. This paper mainly discusses the design and development of data acquisition

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system based on FPGA, and its main function is AD voltage acquisition. Through the design of the board and the debugging of the hardware circuit and control logic can be obtained to meet the requirements of the design.

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